東海大學電機工程學系

碩士論文

使用多相位展頻技巧抑制電磁干擾之降壓型穩壓器單晶片設計

Optimized EMI Reduction through Multi-phase Spread-Spectrum Clock Generator Designed for Buck Converter

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考試委員審定書

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使用多相位展頻技巧抑制電磁干擾之降壓型穩壓器單晶片設計，經本考試委員會審查，符合碩士資格標準。

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中 華 民 國 106 年 01 月 13 日

致謝

感謝實驗室的學弟智凱、育彰、冠州的平日的照顧，使得在枯燥的實驗室生活多采多姿。也感謝翁峻鴻老師對小女子的諄諄教誨，視每位學生親生孩子是您對教育的熱情。

摘要

為消除在降壓型交換式轉換器系統之脈衝寬度調變產生器的電磁干擾，本論文提出以多重相位展頻方式結合交錯式降壓型轉換器，其以多重相位展頻調變方式實現。

一般具有脈衝寬度調變產生器之交換式轉換器，當交換式轉換器開啟到達穩態之時,其開關不斷切換所造成的諧波嚴重導致電磁干擾的問題，進而影響到周圍電路的工作，嚴重則將降低效率。

此展頻技術是藉由數位類比轉換器控制從五十萬赫茲到八十萬赫茲的調變頻率，分別控制 90°相位差的三角波。此外，結合多相位交錯式交換式轉換器更能有效抑制電磁干擾並使其最佳化。本論文分成三大部分，第一部分為簡要介紹降壓型交換式轉換器和展頻調變的原理；第二部分將詳細說明關於多相位展頻產生器與多相位交錯式降壓轉換器的整體概念；第三部分則是著重在電路的實現，包含子電路的細節分析，以及模擬與量測結果。此晶片是以 TSMC 0.18μm製程製作，總體佈局面積為 1.15 x 1.19 mm2，而在量測結果上在電磁干擾方面有著高達 21dB 的抑制效果。

Abstract

In this work we present a multiphase spread-spectrum frequency modulation (multiphase SSFM) to diminish EMI using a multiphase spread-spectrum clock generator (multiphase SSCG) in multi-interleaving PWM buck converter.

In general PWM switching converters, switching noise and harmonic noise causes excited ripple voltage resulting in EMI emission as buck converter reaches steady state. EMI will result in seriously interfering surrounding equipment and thus interrupting its operation, and furthermore, decreasing efficiency.

The proposed SSFM technique is implemented by means of interleaving quadrature triangular waves, which is accomplished by means of DAC varying switching frequency between 500kHz and 800kHz. In addition, with a multi-interleaving PWM buck converter will obtain optimizing amplitude reduction of harmonic interference. There are three major parts in this paper. The first part describes brief introduction of PWM buck converter and SSFM. The second part elaborates on the concepts of multiphase SSCG and multi-interleaving PWM buck converter. The significantly third part demonstrates the implementation of the proposed circuit in detail, including simulations of subcircuits and measurement of the chip. The circuit is fabricated in TSMC CMOS 0.18μm technology and the whole chip area occupies 1.15 x 1.19 mm2, showing a significant 21 dB EMI reduction in the conducted EMI disruptions.

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CHAPTER 1

INTRODUCTION AND BACKGROUND

1.1 BACKGROUND AND REVIEW

More and more portable devices require smaller and lighter due to fast development of manufacturing process. We can find out that there are lots of electrical products in human's life such as ipod, PDA, digital camera, GPS device and smart phone. To improve efficiency and development of green energy, high regard of power management system must be took for granted.

1.2MOTIVATION

In power management system, common methods for controlling switching regulator are Pulse Width Modulation (PWM) and Pulse Frequency Modulation (PFM). Employing switching regulator causes a serious problem in EMI. Thus, a technique of Spread Spectrum Frequency Modulation (SSFM) in the recent year has been proposed.

1.3 WHAT IS EMI?[1]

There are many forms of electromagnetic interference. EMI can affect circuits and prevent them from working in the way that was intended. EMI can arise from many sources which can have a variety of characteristics dependent upon its source and the nature of the mechanism giving rise to the interference. It consists conducted emissions and radiated emissions. The former is the one which conducts through wire of each adjacent equipment, or

from a PCB board when integrated chips have been operated in gradually increasing frequency in recent years.

By the very name of interference given to it, EMI is an unwanted signal at the signal receiver, and in general methods are sought to reduce the level of the interference.

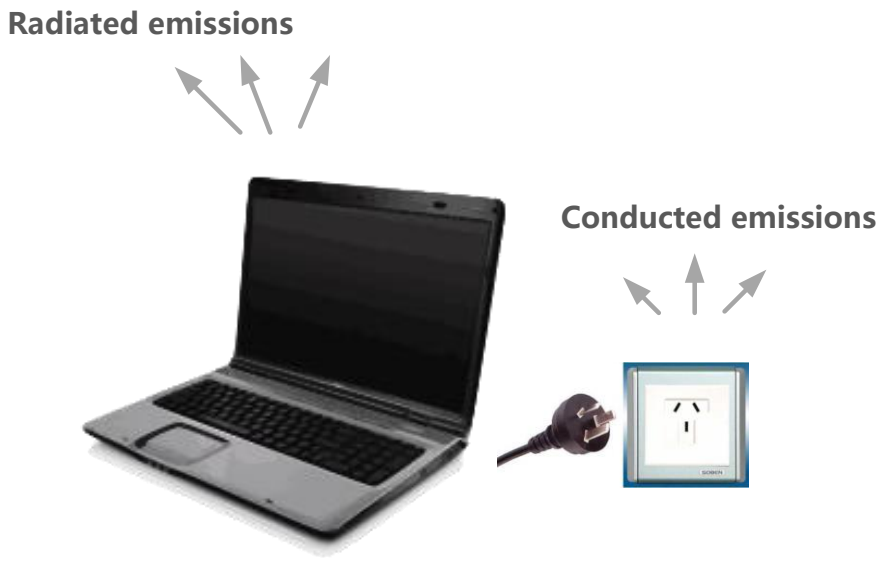


Fig.1.1 Illustration of EMI emissions types

1.4 SOLUTIONS TO EMI CONDUCTION

1.4.1 ELECTROMAGNETIC SHIELDING

Electromagnetic shielding is the usage of surrounding conductive metals to guard against incoming or outgoing emissions of electromagnetic frequencies (EMF). The shielding can decline effectively the coupling of electromagnetic fields and electrostatic fields. However, this way can be a heavy and bulky solution to entire designs although it is

effective and easy to implement. Also, it will substantially increase the cost. Therefore, it is not suitable in recent years for the portable device which has been pretty popular.

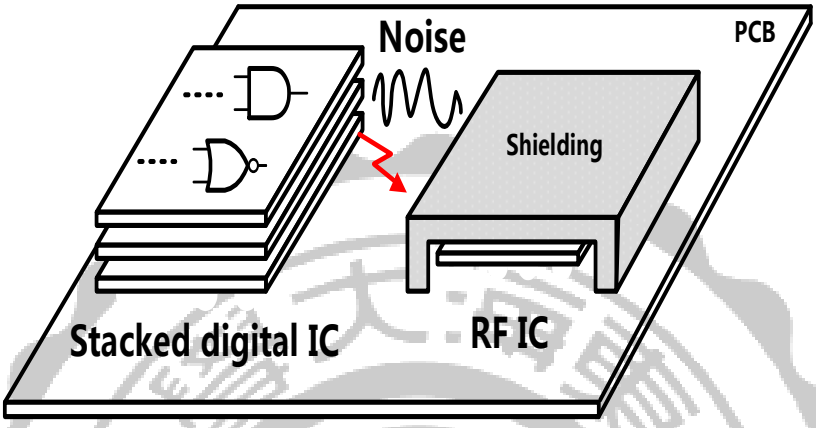


Fig.1.2 Illustration of electromagnetic shielding

1.4.2 PASSIVE SNUBBER CIRCUITS

Snubber circuits are employed by means of passive elements to achieve suppression of EMI emission. Generally, the high side MOSFET is connected to snubber circuits in series while the low side MOSFET is paralleled by the one. The advantages of using snubber circuits not only can eliminate the voltage and current spikes but also can reduce EMI by damping voltage and current ringing. However, though the usage of snubber circuits make the system tend to not so complicated, it will result in extra area being waste on PCB just as the technique of electromagnetic shielding.

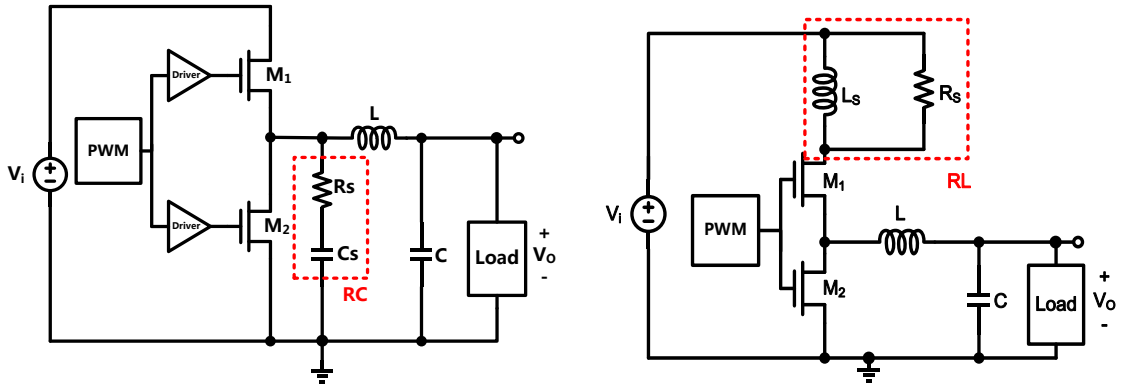


Fig.1.3 An illustration of passive snubber circuits

1.4.3 SPREAD SPECTRUM FREQUENCY MODULATION (SSFM)

SSFM is a technique that controls frequency of the PWM signals modulated between the selective frequency ranges.[2] Employing SSFM technique can efficiently reduce the magnitude of the harmonic.[3] That is to say, the magnitude of the carrier frequency would be reduced and consequently broaden the frequency bandwidth among average distribution. Fig.1.4 is the illustration of the description we stated. SSFM could make the system organization be complicated and the layout area increase.

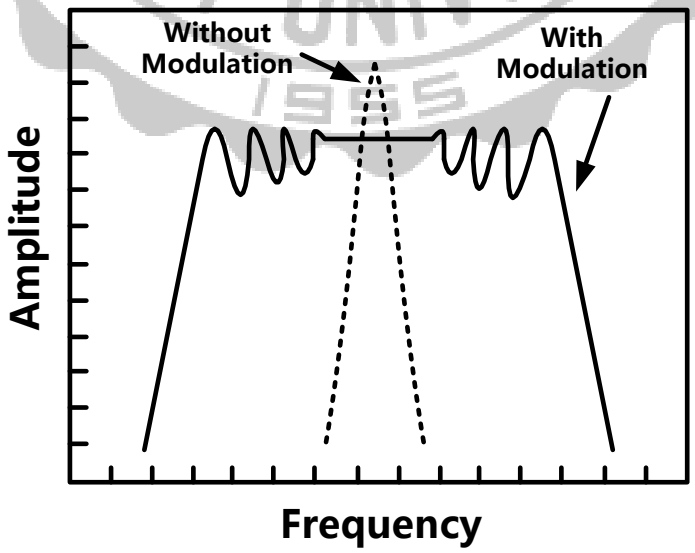


Fig.1.4 Comparison of the harmonic with modulated and without modulated

1.5 THESIS ORGANIZATION

In this thesis, an Optimized EMI Reduction through Multi-phase Spread-Spectrum Clock Generator Designed for Buck Converter is proposed. There are six chapters elaborated on

In Chapter 1, owing to rise of switching frequency in power IC, issue of EMI become more and more popular discussed. Therefore, simplicity of EMI and lists several solutions to EMI reduction is introduced.

In Chapter 2, a principle of SSFM will be discussed in detail while a concept about interleaving technique in Chapter 3 will be elaborated on. Chapter 4 is proposed to the architecture of the whole system. Each block circuit will be subscribed in detail. Last but not the least, Chapter 5 is the layout and the measurement of this proposed work.

CHAPTER 2

CONCEPT OF SPREAD SPECTRUM FREQUENCY MODULATION

2.1 MODULATION PROFILES[4], [5]

It is crucial to consider about what will bring about difference in distribution of frequency. The modulation profile in time domain makes an influence on distribution of frequency in frequency domain resulting in variation in patterns. In other words, the shape of distribution of frequency depends on the modulation profile. Fig.2.1 illustrates three modulation

profiles which are (a) sinusoidal waveforms, (b) triangular waveforms and (c) exponential waveforms, respectively.

The chosen modulation which takes advantage of its periodic profiles introducing into PWM control circuit is to accomplish SSFM. We can observe from Fig.2.1 (a) (b) (c) that different modulation profile results in difference in the shape of spectrum. In this paper we choose triangular modulation implementing SSFM. The benefit of employing the triangular profile is that the spectrum is well-distributed in peak of amplitude. In addition, the slope of triangular wave can be manipulated linearly so that the quantity of EMI reduction is able to control. Although the sinusoidal profile is much easier to analyze and implement, for the reason of the energy concentrating on corner of the spectrum brings about asymmetric shape, the method does not provide optimum of EMI attenuation.

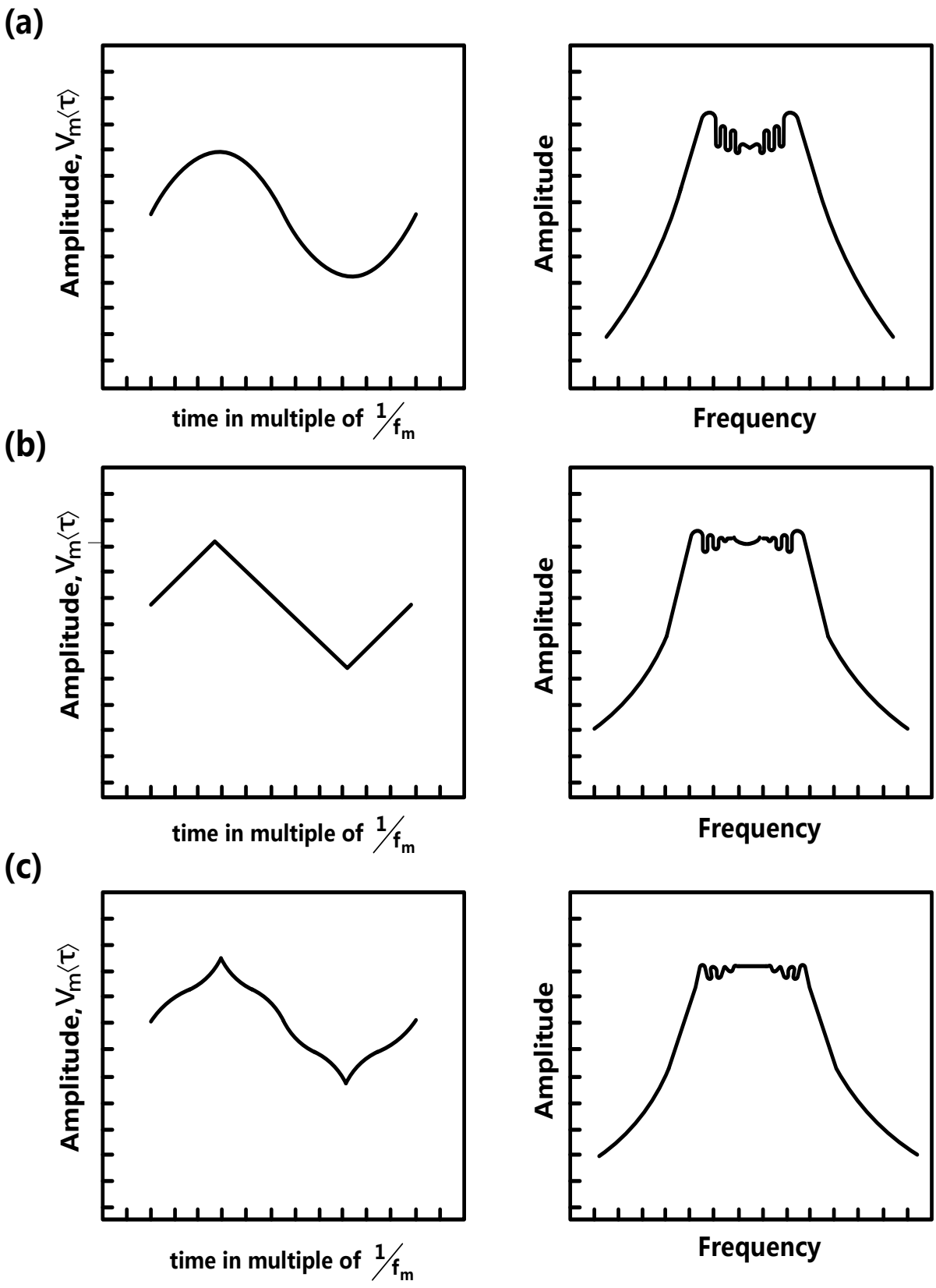


Fig.2.1 Generic modulation profiles.

2.2 PRINCIPLE OF SPREAD SPECTRUM FREQUENCY MODULATION[6]

The generic expression of a modulated waveform can be written as follows:

$$\mathrm{F(t)} = \mathrm{A(t)} \cdot \cos\{\, 2\pi f_c \cdot \mathrm{t} + \theta(\mathrm{t}) \,\}$$

where:

A(t) is a time-dependent amplitude;

f_c ($\omega_c = 2\pi f_c$) the carrier (or switching) frequency;

$\theta(\mathrm{t})$ is a time-dependent phase angle.

$$\theta(\mathrm{t}) = \int_0^t k_w \cdot V_m(\tau) \cdot \mathrm{d}\tau$$

where :

k_w is the factor which controls the peak of frequency deviation;

$V_m(\tau)$ is the modulation profile what we have designated.

Modulation index is defined as:

$$m_f = \frac{\Delta f_c}{f_m}$$

where

Δf_c is peak deviation of the switching frequency;

f_m frequency of the modulation profile function.

The rate of modulation is given as:

$$\delta = \frac{\Delta f_c}{f_c}$$

CHAPTER 3

FUNDAMENTAL OF LOW DROPOUT LINEAR REGULATOR (LDO) AND BUCK CONVERTER

3.1 PRINCIPLE OF LDO

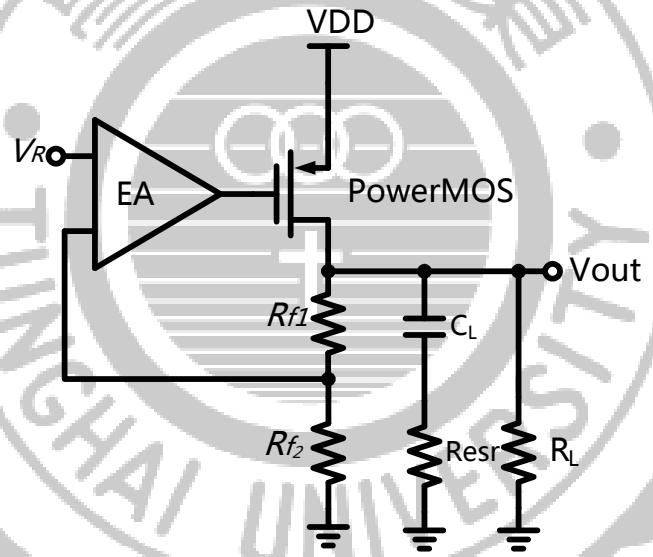


Fig.3.1 An illustration of LDO

The Low Dropout Linear Regulator[7] can be employed in applications that need to drop a higher input voltage to a lower output voltage at relatively appropriate power levels. It is especially proper to use in applications which require low noise, low current and which have a small difference between the input and output voltage. As shown in Fig.3.1, the error amplifier compares

the reference V_R to the feedback voltage which is from V_o divided across two series resistors. The V_o can be controlled from the Eq.

$$V_o = V_R \times \frac{R_{f2}}{R_{f1} + R_{f2}}$$

where R_{f1}, R_{f2} are series resistors of the feedback network.

3.2 PRINCIPLE OF BUCK CONVERTER[8]

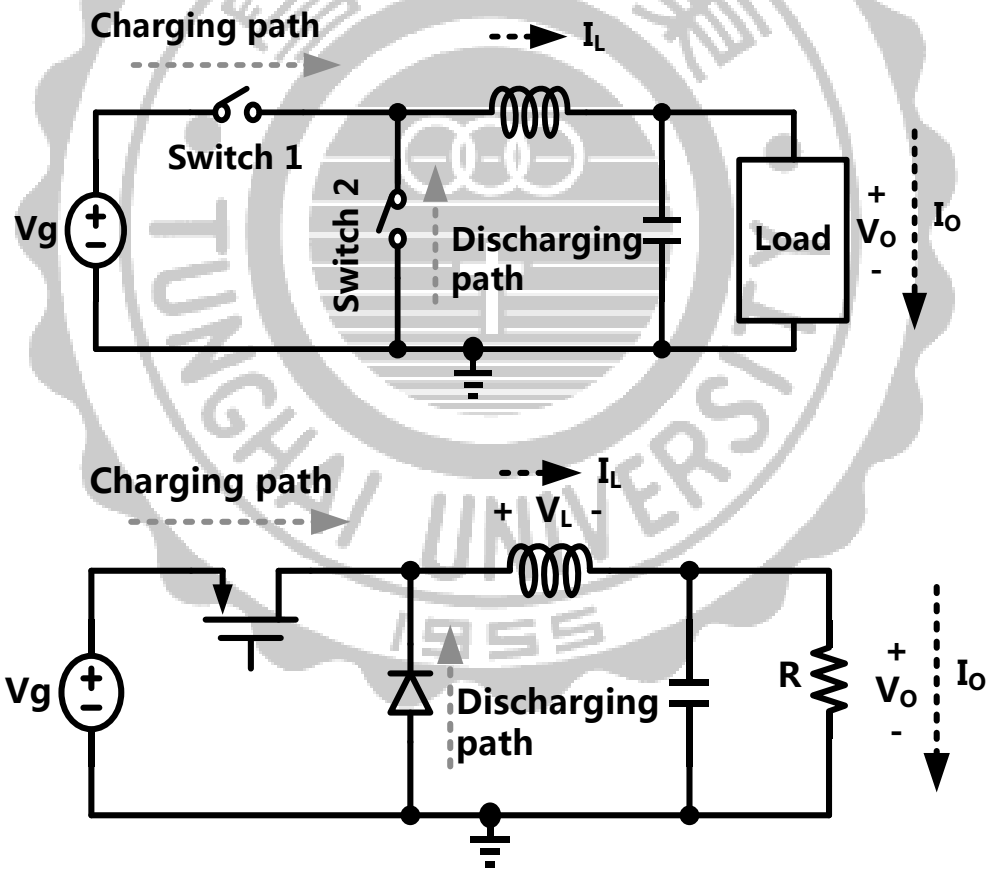


Fig.3.2 Illustration of Buck Converter

As shown in Fig.3.2, as switch 1 is ON (P-type PowerMOS is saturated), the source V_g flows to the load. At this moment the current goes through the inductor resulting in instantaneous voltage drop. However, the current of inductor increases linearly and arises electrical magnetic field, and at the same time the output voltage V_O at the load R is produced. Furthermore, the switch 2 is OFF (as diode is reversed) and the capacitor is charged. In the other state, as switch 1 is OFF (P-type PowerMOS is cut off), the storage of the inductor releases. At this moment, the polarity across the inductor changes direction thus the diode is forward-biased which make the capacitor discharge. The current of the inductor decreases and delivers the storage to the load R leading to an output voltage $-V_o$.

3.2.1 CONTINOUS CONDUCTION MODE

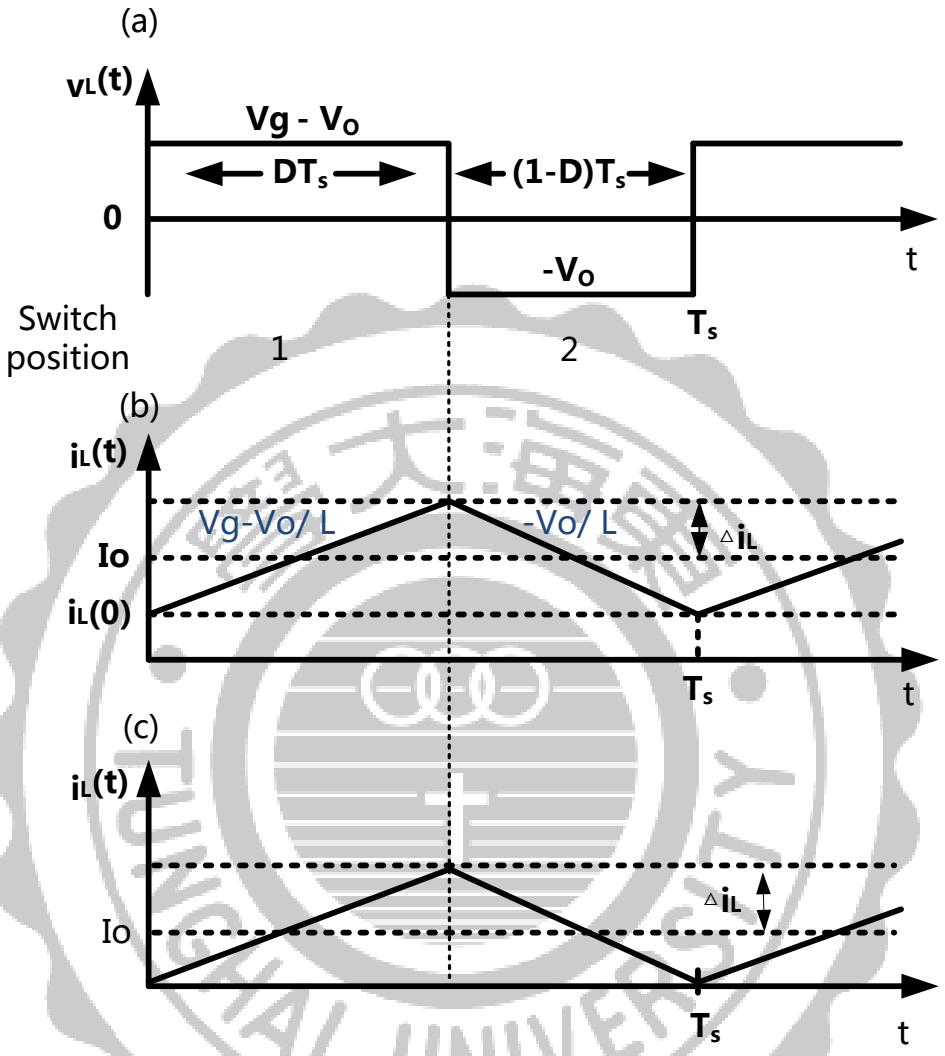


Fig3.3 Illustration Inductor current during CCM

In this state, the current of the inductor never goes to zero and keeps continuous between switching cycles. As a result, there are only two working states in every period as shown in Fig3.3 (a). The first subinterval is when the switch 1 is ON, by knowledge of the inductor voltage definition is

$$v_L(t) = L\frac{di_L(t)}{dt} \quad (2.1)$$

In other words, the inductor current can be found by use of the definition

$$\frac{di_L(t)}{dt} = \frac{V_g - V_o}{L} \quad (2.2)$$

Next, as the switch 2 is ON, similar arguments apply in the second subinterval. Eq. (2.2) leads to

$$v_L(t) = -V_o \quad (2.3)$$

Replacing the Eq. (2.3) into Eq. (2.1) yields

$$\frac{di_L(t)}{dt} = -\frac{V_o}{L} \quad (2.4)$$

According to Eq.(2.2) and Eq.(2.4), the inductor current waveform can be sketched illustrated by Fig.3.3 (b) The inductor current increases when the switch 1 is ON. At t = DT_s, the inductor current then decrease within the switch 2 is ON. The switch 1 changes back to be ON as t = T_s and the process repeats.

Since we know the slope of the inductor current ripple Δi_L and the length of subinterval from the Fig.3.3 (a), Eq. (2.5) can be obtained thus determine the Δi_L and L.

$$2\Delta i_L = \frac{V_g - V_o}{L} DT_s \quad (2.5)$$

3.2.2 DISCONTINOUS CONDUCTION MODE

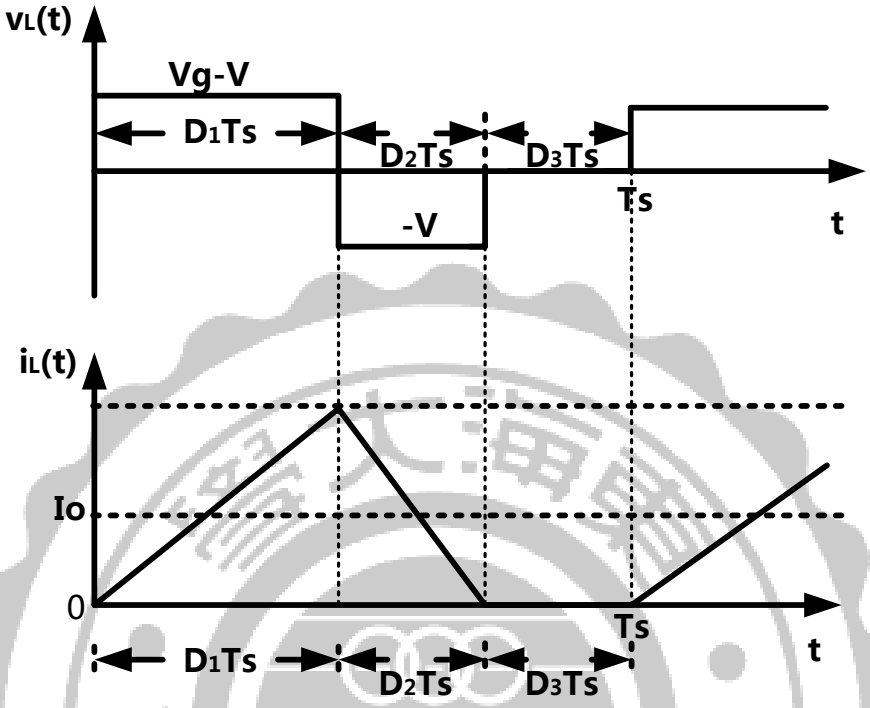


Fig3.4 Illustration Inductor current during DCM

Assume that the load R is increased, and then the dc current I_o is decreased. As I_o declines to Δi_L, here the boundary conduction mode is. Fig3.3(c) shows the boundary conduction mode about inductor current. The switching ripple peak amplitude is:

$$\Delta i_L = \frac{V_g - V_o}{2L} DT_s = \frac{V_g DD' T_s}{2L} \quad (2.6)$$

From Eq. (2.6) can understand that the inductor current magnitude not depends on the load R. If we continue to increase R, because the diode current would not be negative, there will be three subintervals during each switching period T_s as shown in Fig3.4. There is the condition for operation follows:

$$I_o > \Delta i_L \text{ for CCM}$$

$$I_o < \Delta i_L \text{ for DCM (2.7)}$$

where I_o and Δi_L are found assuming that the converter operates in the discontinuous conduction mode. Insertion of $I_o = \frac{V}{R}$ and Eq. (2.6) into Eq. (2.7) yields

$$\frac{DV_g}{R} < \frac{V_g D D' T_s}{2L} \text{ (2.8)}$$

Simplification leads to

$$\frac{2L}{RT_s} < D' \text{ (2.9)}$$

Thus, the boundary mode between continuous and discontinuous mode of the load R can be defined as

$$R_{crit} = \frac{2L}{D'T_s} \text{ (2.10)}$$

which can expose directly mode:

$$\text{R} < R_{crit} \text{ for CCM}$$

$$\text{R} > R_{crit} \text{ for DCM.}$$

3.2.3 THE BASIC INTERLEAVING CONCEPT[9]

Owing to the fact that the popularity of power management IC has been researched and developed in recent years, the related interfering factor such as EMI affecting efficiency has been high regarded. Interleaving technique takes advantage of paralleled current interleaving in quadrature phases. We can see the configuration in Fig.3.5 From $I_{0(t)}$ to $I_{N-1(t)}$ are interleaving currents, respectively.

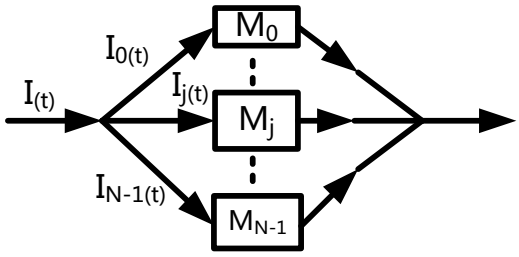


Fig.3.5 Configuration of interleaving concept

According to Kirchhoff's current law, we can get the sum of interleaving current every phase, respectively. [10], [11]

$$I(\mathrm{t}) = \sum_{j=0}^{N-1} I_{j(t)}$$

However, there will be a discussion if we introduce $I_{0(t)}$ to $I_{N-1(t)}$ as the same frequency as $I_{(t)}$. A calculation for the magnitude of the inductor current in terms of Fourier is proposed:

$$I_p(t) = \sum_{n=-\infty}^{n=+\infty} \mathrm{c_n} \cdot e^{-j\cdot 2\pi\cdot p\frac{n}{M}}$$

Where n is the nth harmonic. Total current is the sum of current through M phases.

$$\mathrm{c_n}|_{total} = \sum_{p=0}^{M-1} \mathrm{c_n} \cdot e^{-j\cdot 2\pi\cdot p\frac{n}{M}} = \mathrm{c_n} \cdot \sum_{p=0}^{M-1} e^{-j\cdot 2\pi\cdot p\frac{n}{M}}$$

Take $\sum_{p=0}^{M-1} e^{-j\cdot 2\pi\cdot p\frac{n}{M}}$ term for operation, we obtain that if $\frac{n}{M}$ is not integer, $c_n|_{total}$ will be equal to 0. Conversely, if $\frac{n}{M}$ is integer, the $c_n|_{total}$ will be M times of c_n.

$$c_n|_{total} = c_n \cdot M \quad \text{if } \frac{n}{M} \in Z$$

$$c_n|_{total} = 0 \qquad \text{if } \frac{n}{M} \notin Z$$

Obviously, from Eq. the multiple of nth harmonic would be concentrated and others would be cancelled. For instance, if we set the switching frequency as 500k with interleaving four phase, frequency of 500K Hz,1M Hz and 1.5M Hz which convert to harmonics will be cancelled but still the 2M Hz one exists. Therefore, if we interleave M-paralleled module, every module are shifted by $2\pi/M$ and the frequency f of I(t) will be M times of $I_{j(t)}$. As a result, in order to solve this problem, frequency f of $I_{j(t)}$ must be set up as f/M so that the frequency of $I_{(t)}$ will be the original one we assume.

Interleaving techniques[12] can substantially reduce EMI which is mainly caused by pulsating signal of PWM generator. To make basic concept of interleaving techniques easy, simple configuration is showed in Fig3.6 which is a dual converter comprising two inductors and one capacitor. The signal through each inductor in synchronous operation with 180 degrees of phase difference constructs composite waveform which is current ripple I_{Ltot}(In other word, it is the sum of current ripple waveforms of L1 and L2). Comparing non-interleaved with interleaved operation as shown in Fig.3.6 (a)(b), peak-to-peak amplitude of the I_{Ltot} in interleaved operation obviously

lower than non-interleaved one, and most important of all, lower than original current ripple I_L. One the contrary, the composite ripple peak-to-peak amplitude of non-interleaved operation will be twice larger than original one I_L.

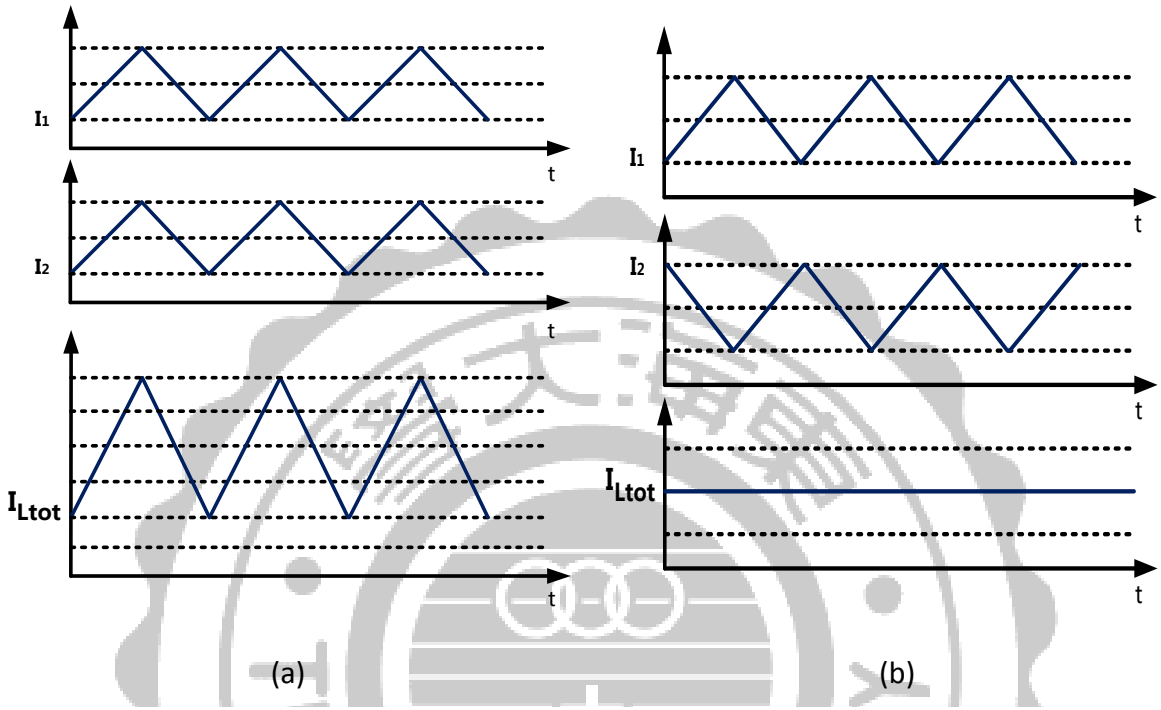


Fig.3.6 Configurations of sum of current ripple waveforms with (a) Non-interleaved (b) Interleaved.

CHAPTER 4

CIRCUITS DESIGN AND ANALYSIS

4.1 SPREAD-SPECTRUM FREQUENCY MODULATION WITH A MULTIPAHSE MULTI-INTERLEAVING BUCK CONVERTER

In this chapter, we will elaborate on evaluation of switching period with shift delays about interleaved PWM signals that is non-modulated and modulated compared with[13]. A general interleaved PWM signal illustrated as Fig.4.1 (a) Every period of PWM signal ($\mathrm{P1}(t), \mathrm{P2}(t), \mathrm{P3}(t), \mathrm{P4}(t)$) whose shift delay is a constant value T_P/N, where N is the N-paralleled converter, integrates with each other into a constant period T_P (S(t)). However, as the period is modulated, the shift delay will not be a constant. Thus we introduce a simple formula $\eta_{x,y}$ in modulated mode.

$$\eta_{x,y} = \frac{T_P{}'}{N}(y-1) \qquad y = 1, 2, 3 \ldots\ldots, N$$

The η_x represents the first pattern equal to 0 and is a constant. After that, $\eta_{x,y}$ varies in modulated period relying on $T_P{}'$ as shown in Fig.4.1 (b) which corresponds to N = 4.

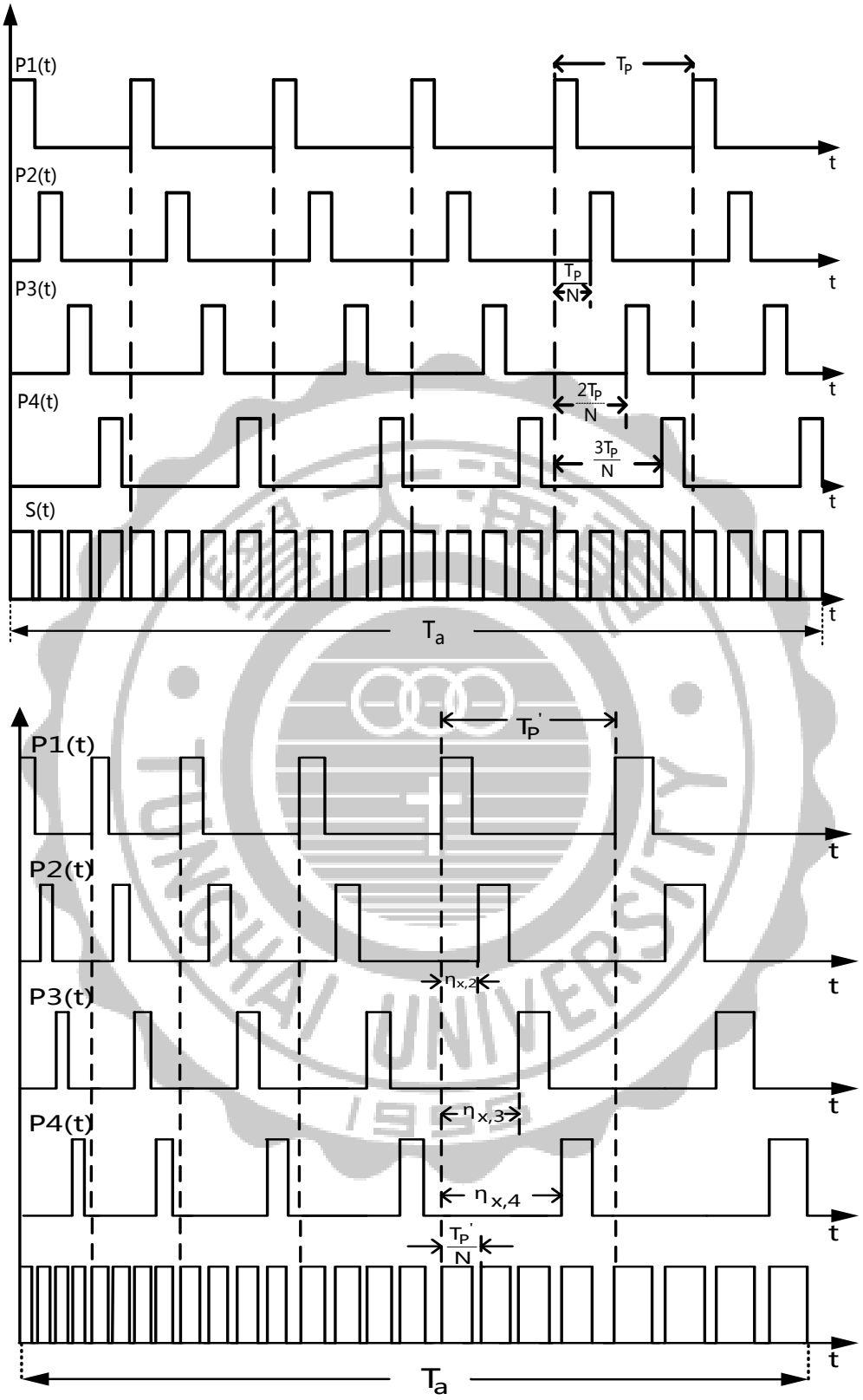


Fig.4.1 PWM signal patterns for N=4. (a) Interleaving (b) Interleaving with SSFM

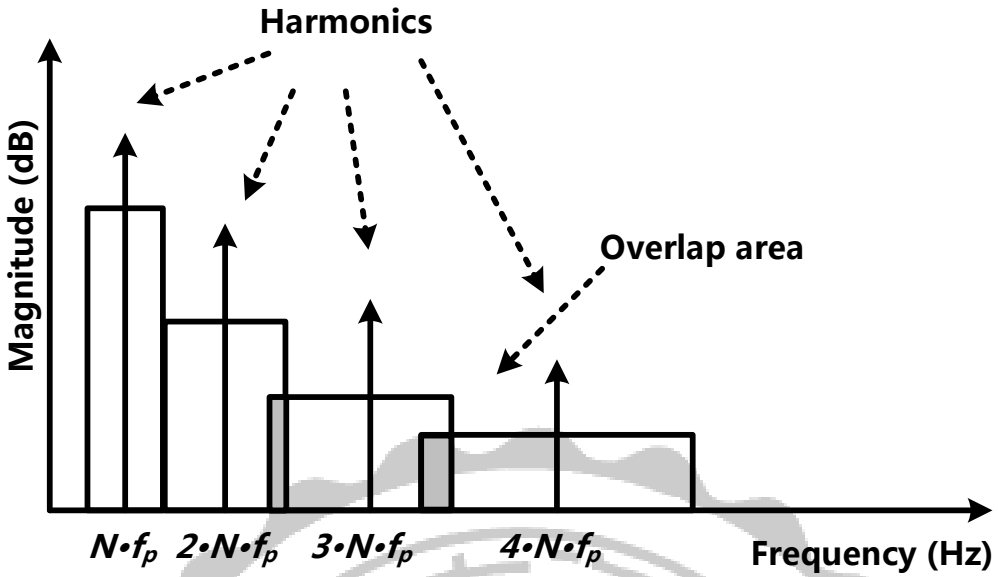


Fig.4.2 Spectrum with SSFM and without SSFM

As interleaving techniques start, PWM signal patterns shift in quadrature phase. Fig.4.2 shows the comparison of EMI spectrum between SSFM is active and not. We can see that the EMI spectra will appears at frequency multiple of N when PWM signals interleave. Next, if the SSFM launches, the original spectra will spread into side-bands harmonics and further the amplitude of EMI spectrum declining.

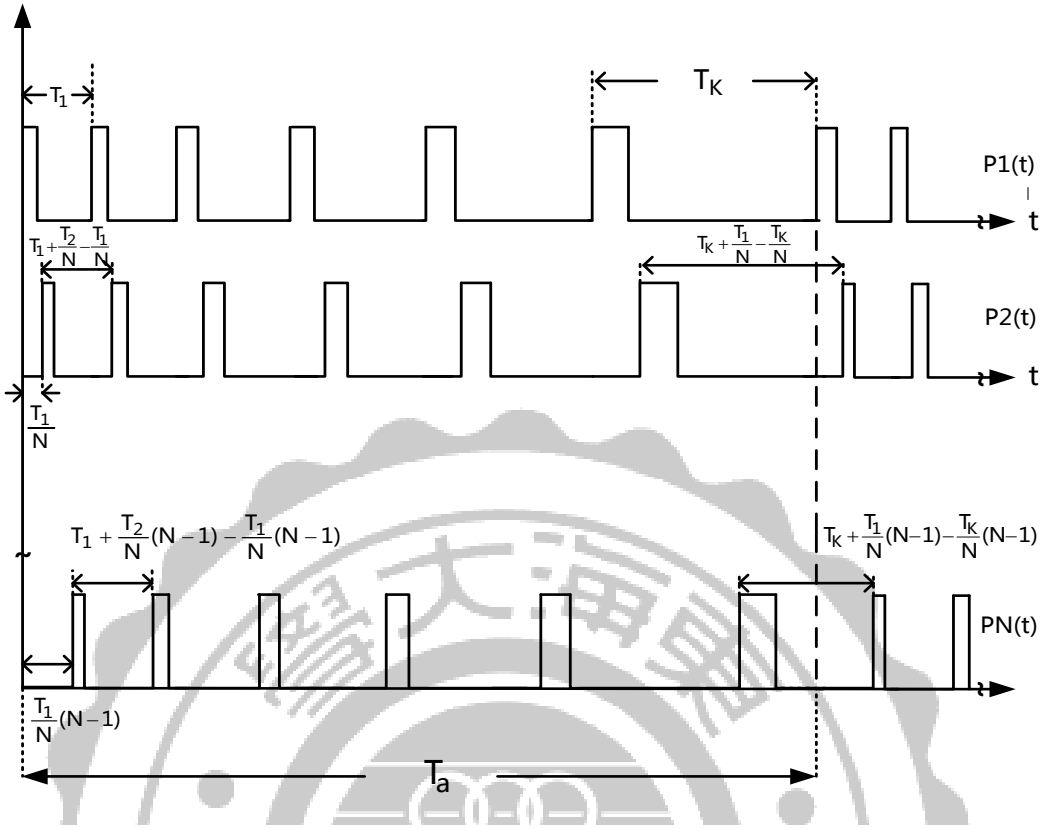


Fig.4.3 Interleaved with SSFM

$$T_{k,i} = T_{k,1} + \frac{T_{k+1,1}}{N}(\mathrm{i}-1) - \frac{T_{k,1}}{N}(i-1) \quad \text{for } \mathrm{k} = \{1,2,3\ldots,\mathrm{L}-1\}$$

$$T_{L,i} = T_{L,1} + \frac{T_{1,1}}{N}(\mathrm{i}-1) - \frac{T_{L,1}}{N}(i-1) \quad \text{for } \mathrm{k} = \mathrm{L}$$

4.2 ARCHITECTURE

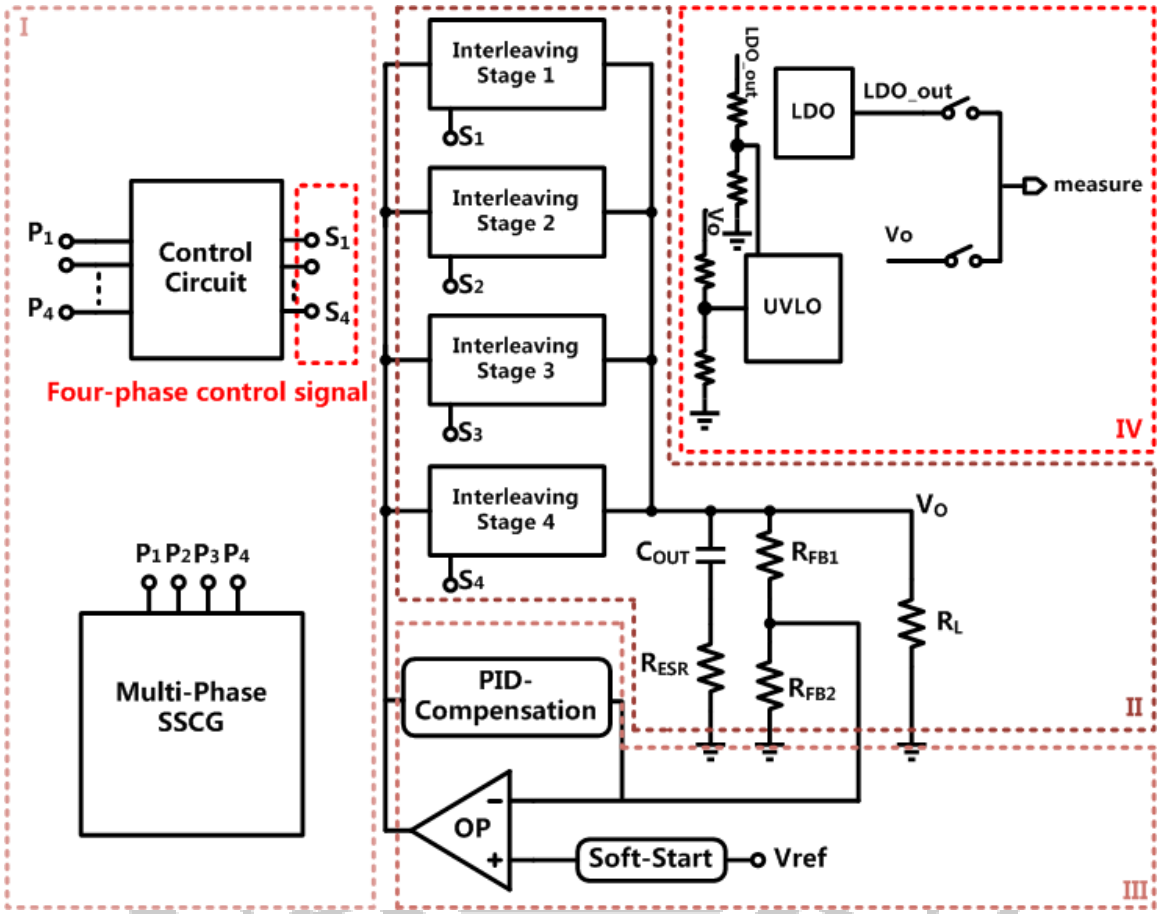


Fig.4.4 An illustration of system organization

Fig.4.4 shows the configuration of entire system. Here are three certain parts separated for analysis. First, the part Ⅰ is Multi-Phase Spread Spectrum Frequency Modulation (Multi-Phase SSFM) which introduces controlling signal to each interleaving circuit for the purpose of urging four quadrature phases achieving the interleaving effect. The Part Ⅱ consists four interleaving circuits and the power stage. Each interleaving circuit is composed of PWM control circuit and PowerMOS as well as an inductor illustrated in Fig.4.5. Each of four interleaving quadrature current ripple flows into the capacitor C_{out} and the resistors R_{FB1} and R_{FB2} which a

feedback voltage of product divided by pulls back to the error amplifier. Then the part Ⅲ includes the error amplifier and PID-Compensation exporting an error voltage that compares with a comparator and then forming PWM signals. Last but not least, part Ⅳ is composed of Linear Dropout Regulator and Under Voltage Lockout Circuit whose mechanism is to make sure the whole system working smoothly and accelerate transient time of regulators.

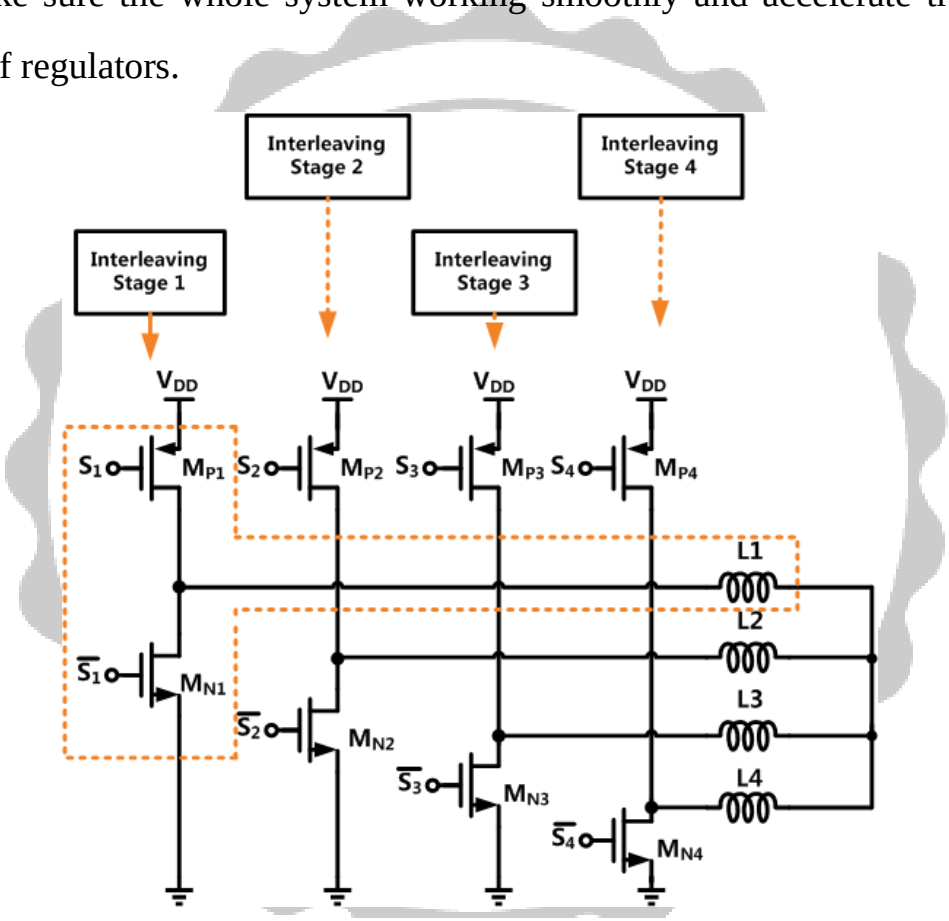


Fig.4.5 Details in Interleaving Stages

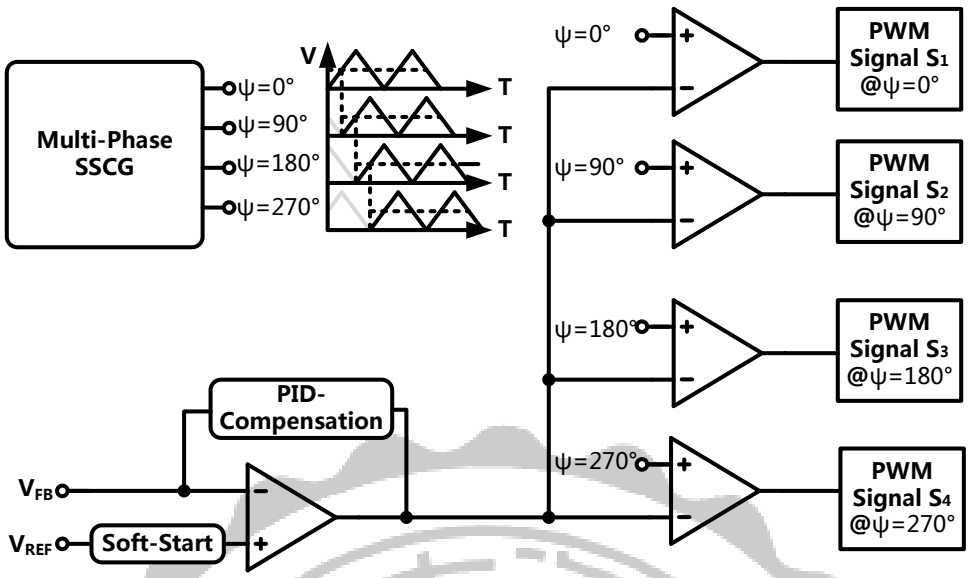


Fig.4.6 Details in interleaving quadrature PWM generator

Fig.4.6 is an illustration of detail in the Control Circuit which the interleaving quadrature PWM generator forms. Multi-Phase SSCG generates quadrature triangular waves introducing into comparators resulting in quadrature square waves as PWM signals. Note that the duty cycle of each square waves is equal but the phase of each is quadrature so that the interleaving techniques can be achieved. Furthermore, the interleaving techniques corresponds Multi-Phase SSCG can realize the whole system we proposed.

4.2.1 PULSE WIDTH MODULATION (PWM) CONTROL CIRCUIT[14]

In this paper, hysteresis comparator and triangular generator constitute this work. The hysteresis comparator determines the switching time of the DC-DC buck converter when the moment at the output state of comparator changes illustrated in Fig.4.7 The PMOSFET turns on charging the inductor

when the V_{TRI} rises to V_C. On the contrary, the PMOSFET turns off and discharges when the V_{TRI} falls below V_C.

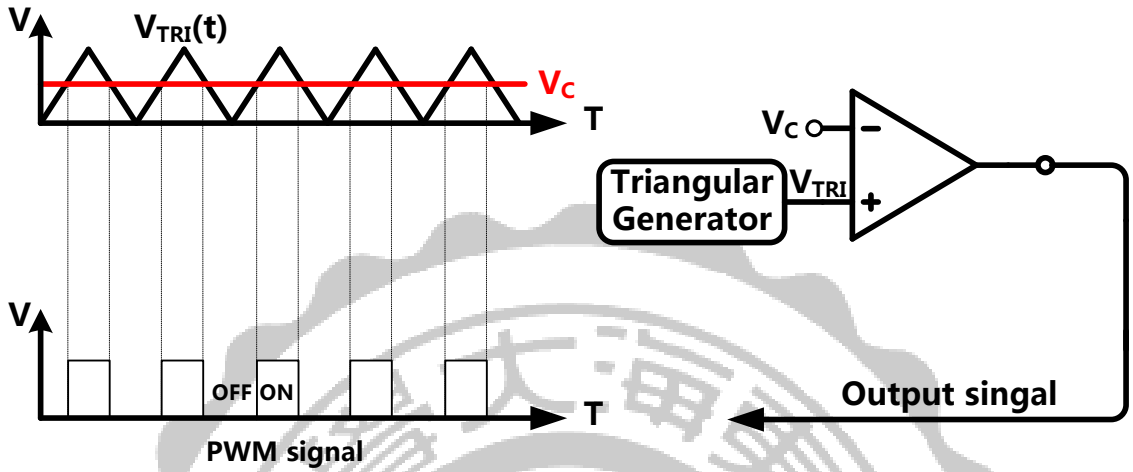


Fig.4.7 Illustration of Hysteresis Comparator

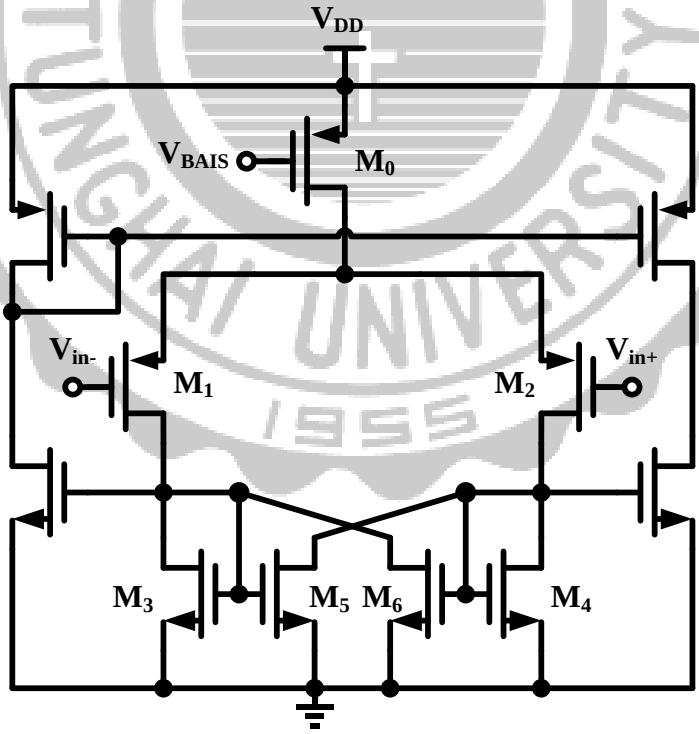


Fig.4.8 Hysteresis Comparator design circuit

If the response time of comparator is much faster than the variation of the input signal around the threshold level, the output will chatter around the two stable levels as the input crosses the comparison voltage. As a result, employing hysteresis comparator is a specific choice.

The comparator used in this design shown in Fig.4.8. It is formed with two stages. The first stage is a p-channel differential input pair with the positive feedback circuit. The second stage is an n-channel differential input pair with a p-channel current mirror active load. As transient simulated shown in Fig.4.9, output delays when V_+ is over V_- will eliminate the chatting effect.

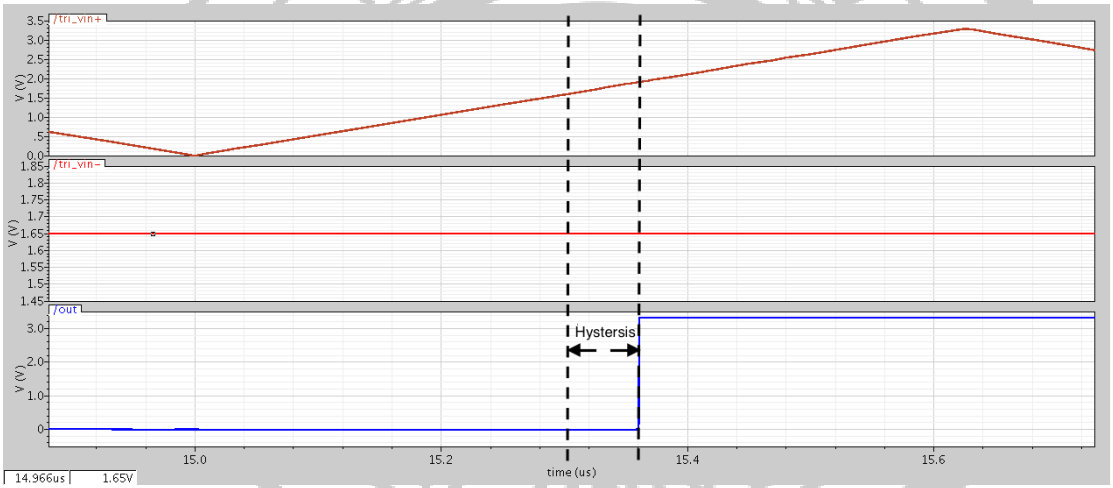


Fig.4.9 Simulation of hysteresis comparator.

4.2.2 NON-OVERLAPPING CIRCUIT[15]

Non-overlapping circuit is also called Dead-time controller. To avoid unnecessary power consumption and elements burnout as power stage (P-type power transistor & N-type power transistor) conducts at the same

time (N1 & N2), a dead-time control circuit is supposed to be added to put off phases of power stage.

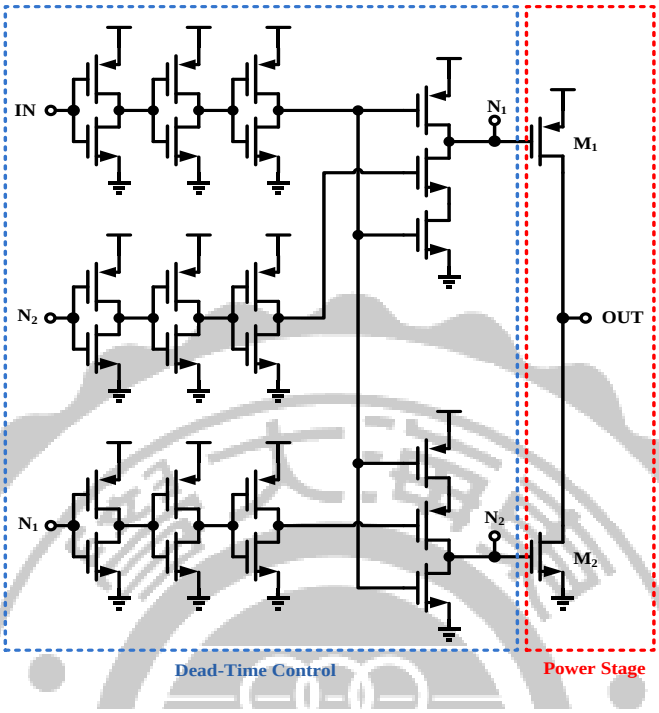


Fig.4.10 Non-overlapping circuit

As simulation for Fig.4.11 , N1 is later than N2

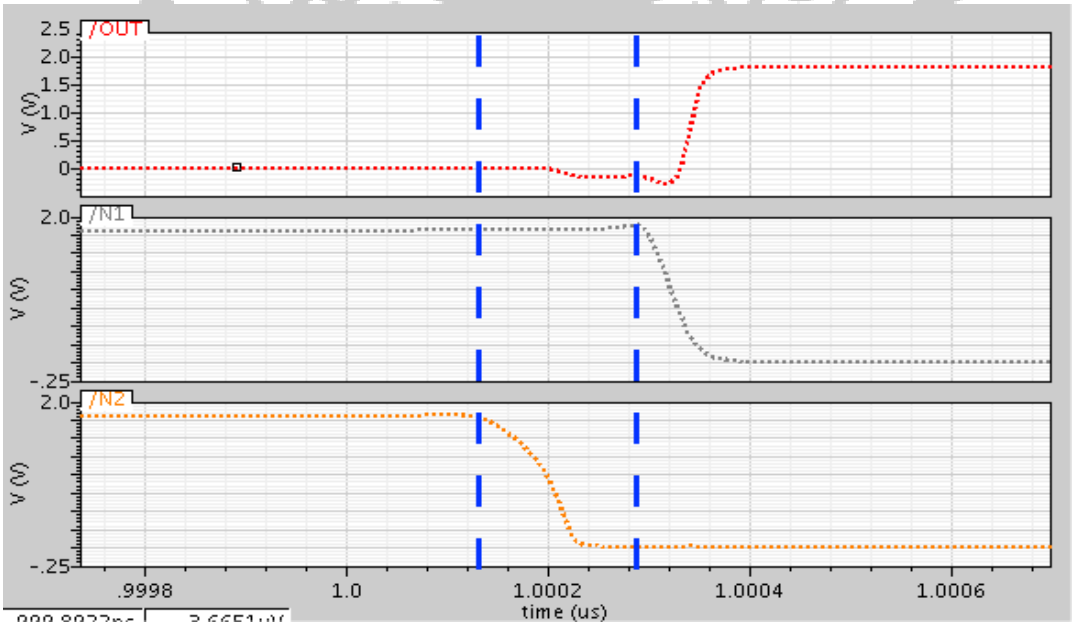


Fig.4.11 Simulation of Non-overlapping circuit

4.2.3 ERROR AMPLIFIER

In this work, a two-stage operational amplifier which is incorporated within PID compensation is employed.[16] The function of Error Amplifier is to compare voltage reference with the negative terminal which is connected to output of voltage division of buck. Thus the error signal can be commensurate with duty cycle generated by the comparator.

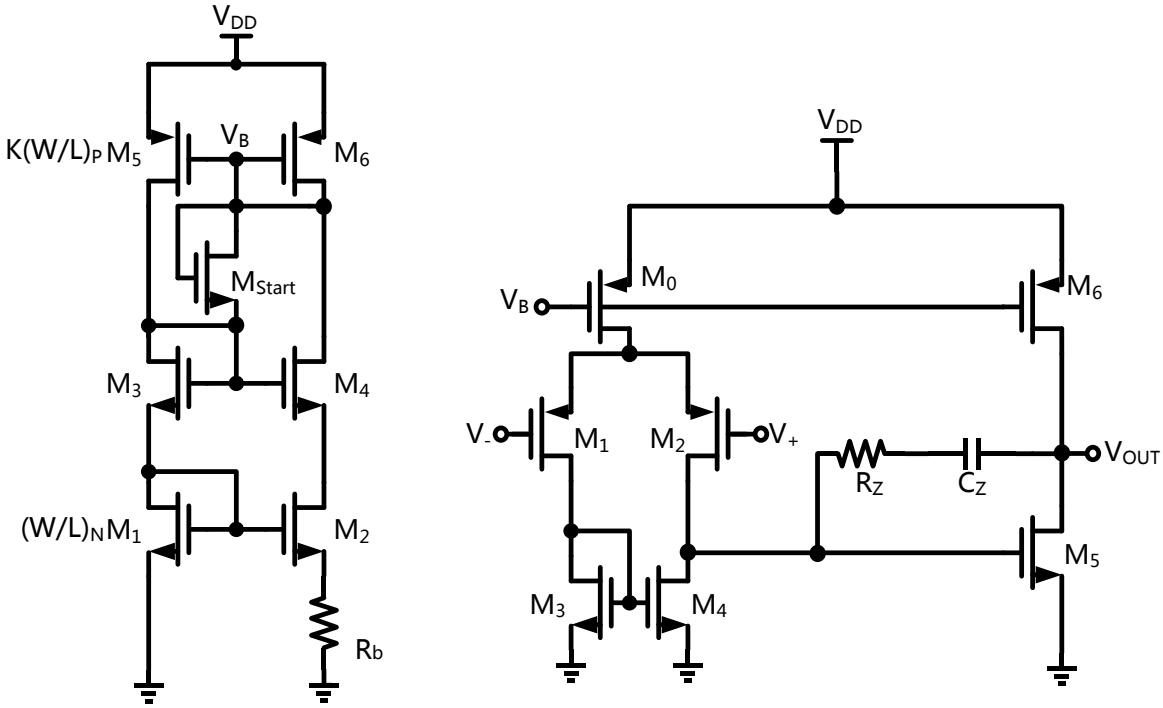


Fig.4.12 Self-bias circuit and Error Amplifier circuit

The first stage is single-ended differential Op-Amp. The second stage is a class-A amplifier. Eq. and Eq. are gain equations of two stages, respectively. For the purpose of maintaining a stable system, sufficient gain and phase margin must be demanded.

$$A_{V1} = g_{m1}(r_{ds2} \,//\, r_{ds4})$$
$$A_{V2} = g_{m5}(r_{ds5} \,//\, r_{ds6})$$

Here we use Self-biased circuit to supply bias voltage. From Eq. we can see that the bias circuit is affected by size of MOSFET excluding supply voltage, temperature, and fabrication parameters.

$$I_{out} = \frac{2}{\mu_n C_{ox}\left(W/L\right)_N} \cdot \frac{1}{{R_b}^2} \cdot (1 - \frac{1}{\sqrt{K}})^2$$

4.2.4 ANALYSIS OF SYSTEM STABILITY

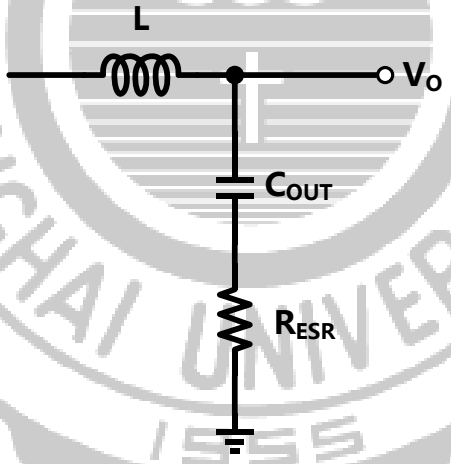


Fig.4.13 Power stage of buck converter

From chapter 2, we elaborated on stability about whole system. A fast transient response with minimal voltage deviation requires an essential principle: an adequate frequency response. Here we continue to discuss details about transfer function of each schematic part. Fig. shows power stage

part and its transfer function is calculated as $T_{pwr}(s)$. From Eq. we understand that there are one zero and two poles.

$$T_{pwr}(s) = \frac{sR_{ESR}C_{OUT} + 1}{s^2LC_{OUT} + sR_{ESR}C_{OUT} + 1}$$

Thus the phase margin would be insufficient resulting in an unstable system. However, a PID-Compensation way could efficiently improve it.

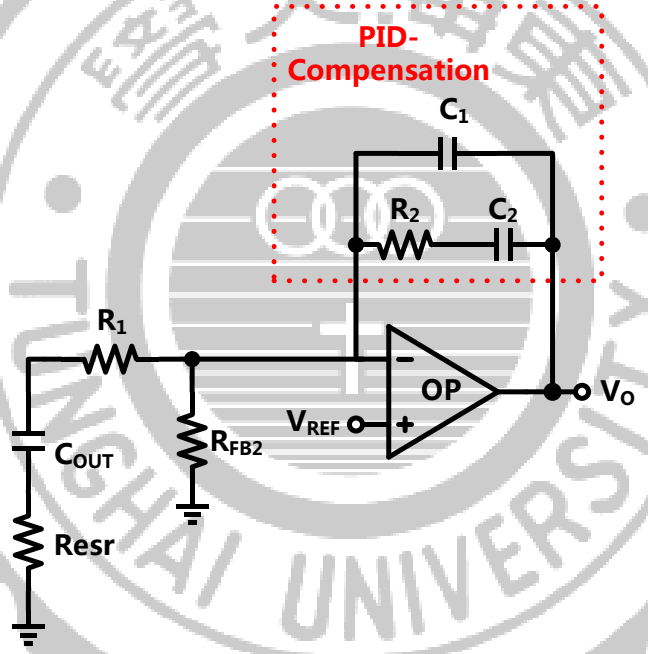


Fig.4.14 Error AMP. with PID-Compensation

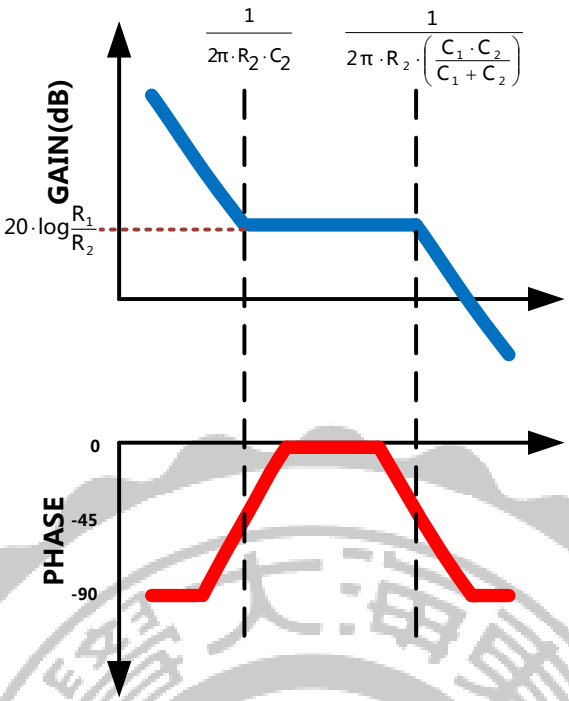


Fig.4.15 Frequency response of Type-II circuit

Fig.4.14 illustrates the Error Amplifier with PID Type-II Compensation. Incorporation with Type-II Compensation could supply zero and pole for the purpose of sufficient phase margin.

$$T_{PID}(s) = \frac{1 + SR_2C_2}{SR_1(C_1 + C_2)(1 + SR_2\frac{C_1C_2}{C_1 + C_2})}$$

The illustration shows in Fig4.15, the zero locates at $f_Z = \frac{1}{2\pi R_2 C_2}$. The first pole locates at $f_{po} = 0$ and the second one locates at $f_P = \frac{C_1 + C_2}{2\pi R_2 C_1 C_2}$. As a result, through this Type-II Compensation not only a 90° provided situates on low frequency band in order to improve phase margin but also a -20dB/decade is provided settling on high frequency band restraining high frequency noise and crossover frequency.

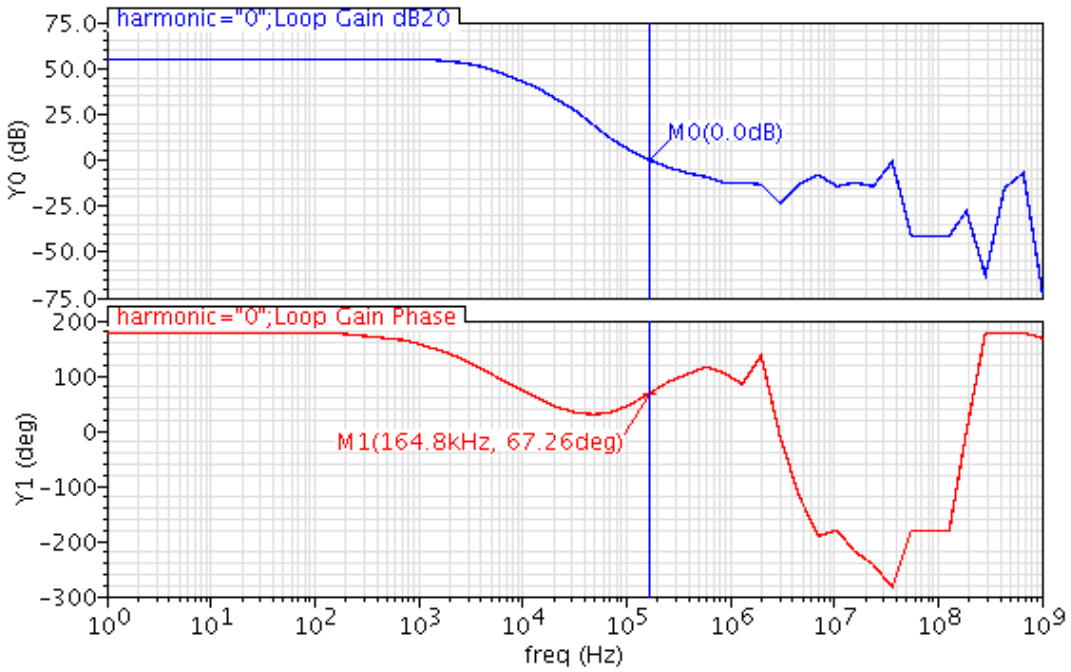


Fig.4.16 Frequency response of loop system

Generally, the crossover frequency is required smaller than 30% switching frequency which prevents interruption from the switching noise. Fig. shows the loop stability by means of PSS and PSTB analysis in Spectre [8]. From simulation can evidently observe whether the loop is stable or not. Table presents every consequence in corner SS, TT, FF, respectively.

Corner	**SS**	**TT**	**FF**
Gain(dB)	55.9	55.27	54.6
Phase Margin	53.79°	66.75°	63.86°
Unity-Gain frequency (kHz)	135.4	163.2	154.8

4.2.5 ZERO CURRENT DETECTOR CIRCUIT[17]

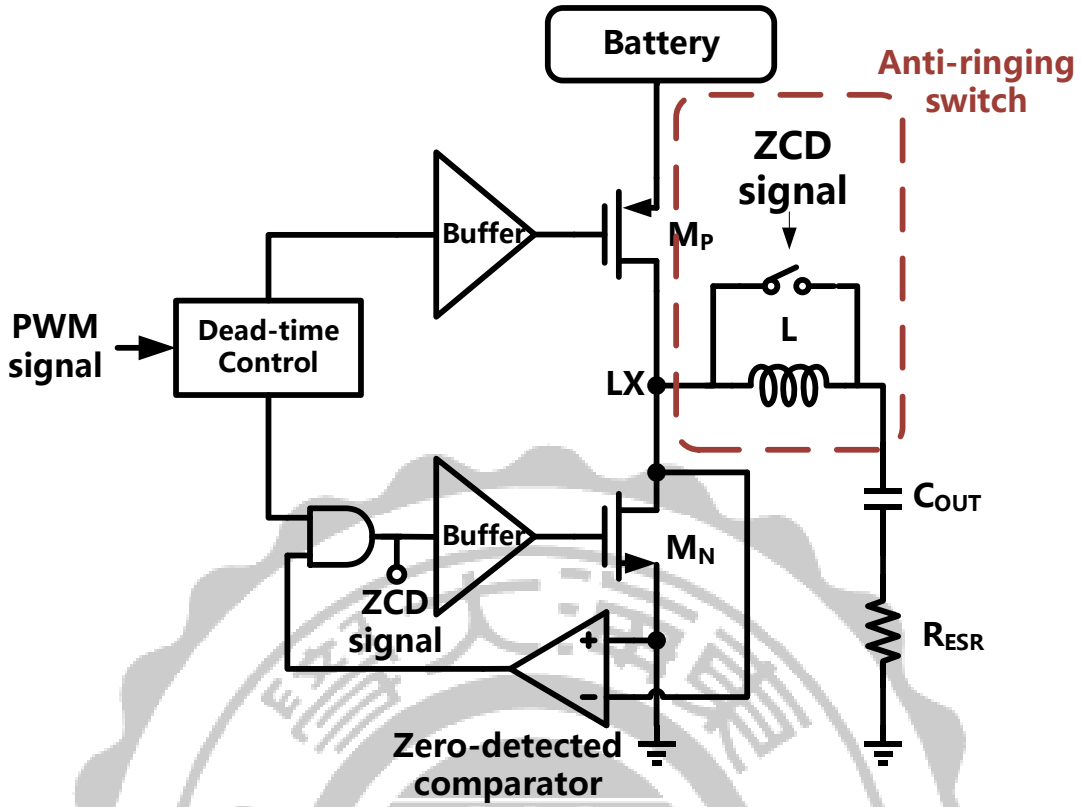


Fig.4.17 ZCD illustration

A diode is employed in asynchronous buck converter which to prevent reverse current in discontinuous condition mode (DCM). Nevertheless, a synchronous buck converter has been supposed owing to power conservation and advance in technique of PowerMOS in the recent year. What is to say that the NMOS plays a role of substitute for the diode. However, when the buck converter is in DCM, the reverse current result in power dissipation by reason of NMOS is unable to block it. To solve this problem, a Zero Current Detector circuit is in need. ZCD is implemented by a Zero-Current Comparator to detect LX if the reverse current happens at the period of the inductor discharging. Once LX decreases below zero volt, the NMOS is switched off that prevents the reverse current from flowing back to the source of NMOS. At the moment that NMOS is turned off, there will be an

oscillation loop between the inductor, capacitor and thus causes oscillation. Therefore, an anti-ringing switch is added to short the inductor by means of ZCD signal controlled as that condition occurs. The following illustrations are simulation of comparison of the device with and without ZCD respectively. As shown in Fig4.18, we can clearly see that V_{LX} displays regular and enormous oscillation if ZCD is not incorporated in. At the same time, large current ripple of inductor result in voltage ripple of V_O and the reverse current occurs in DCM as illustrated in Fig4.20 On the contrary, obviously we can see if ZCD is incorporated in the circuit, the oscillation of V_{LX} disappears and successfully suppresses the reverse current in DCM as shown in Fig.2.1. What is more, the current ripple is in decline which also makes the voltage ripple of V_O decrease as displayed in Fig.4.19.

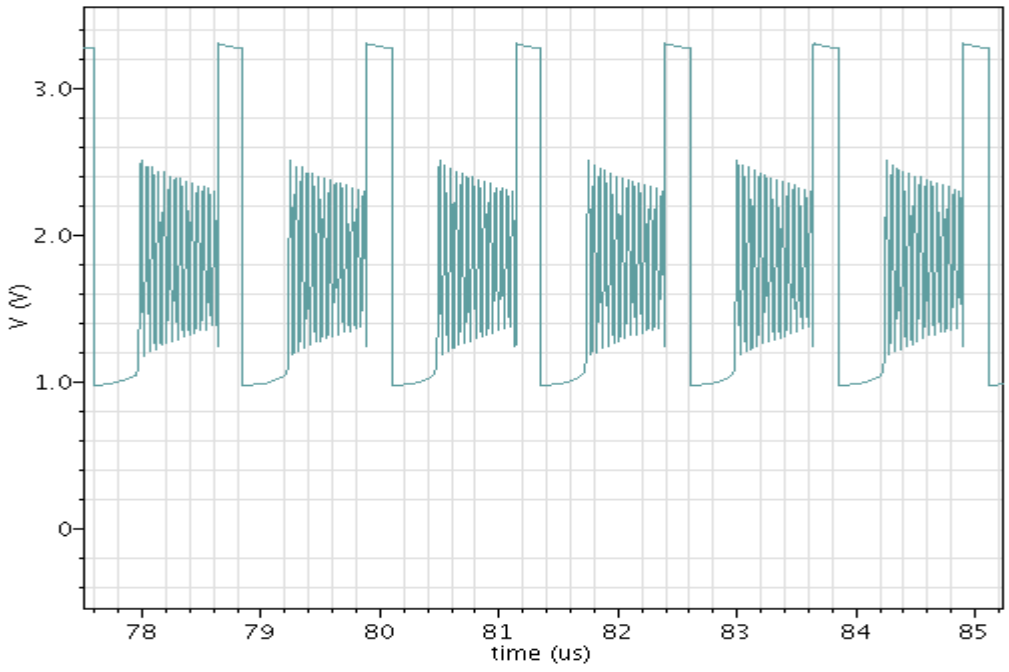


Fig.4.18 Simulations of V_{LX} without anti-ringing switch

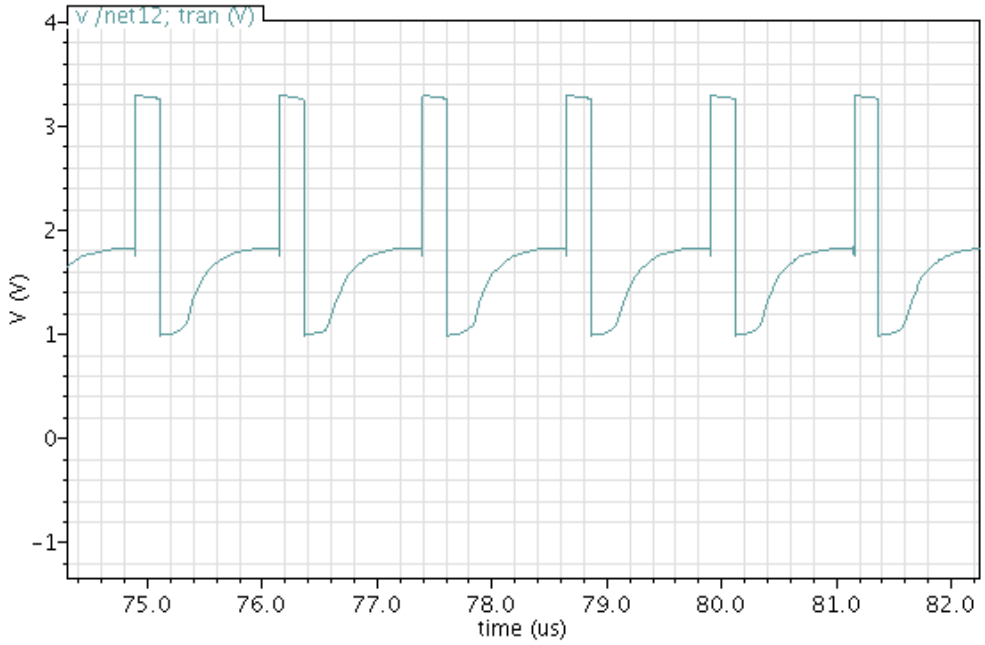


Fig.4.19 Simulations of V_{LX} with anti-ringing switch

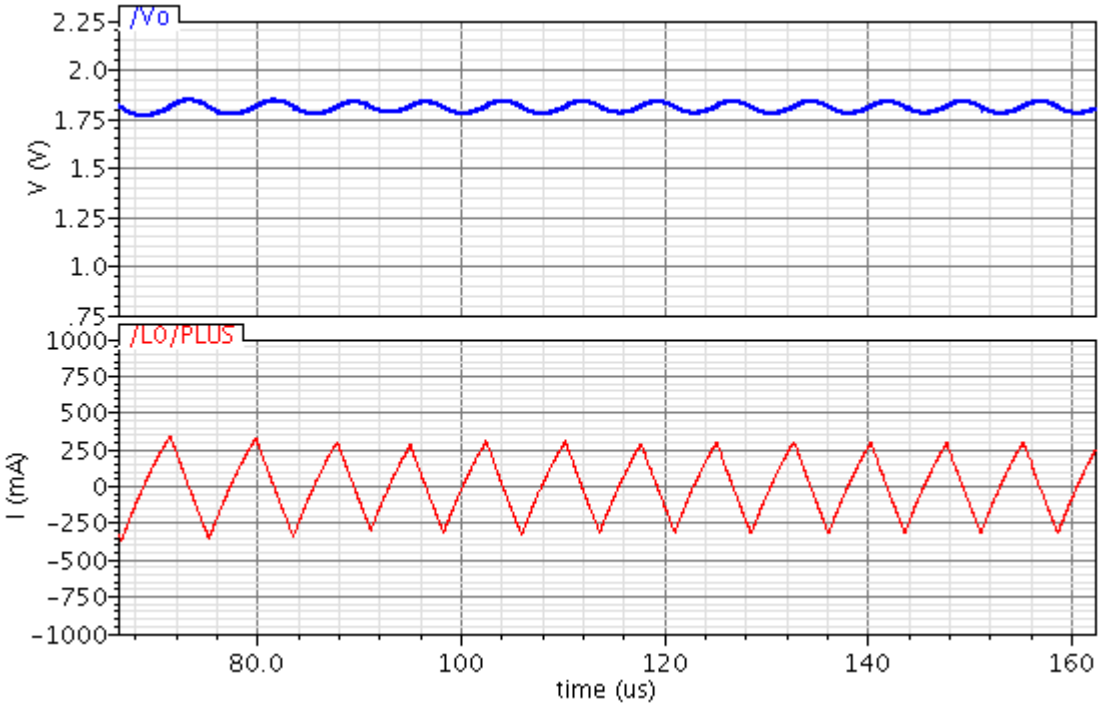


Fig.4.20 Simulations of Vo and I_L of Buck Converter without ZCD

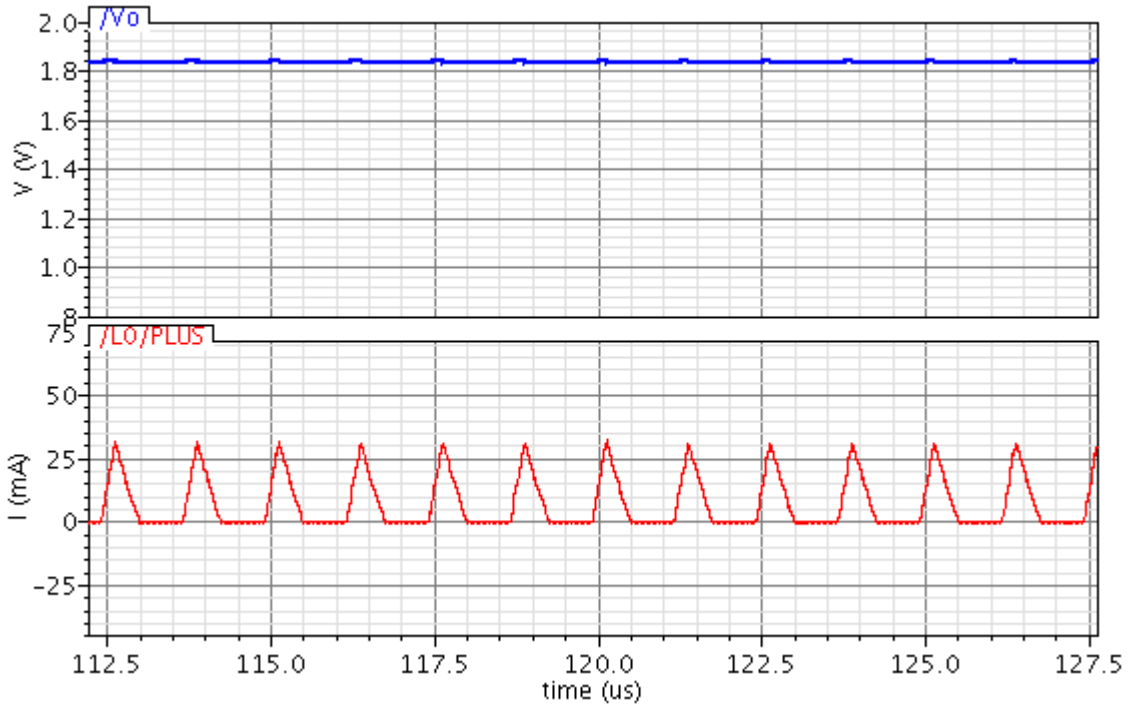


Fig.4.21 Simulations of Vo and I_L of Buck converter with ZCD

4.2.6 SOFT-START CIRCUIT

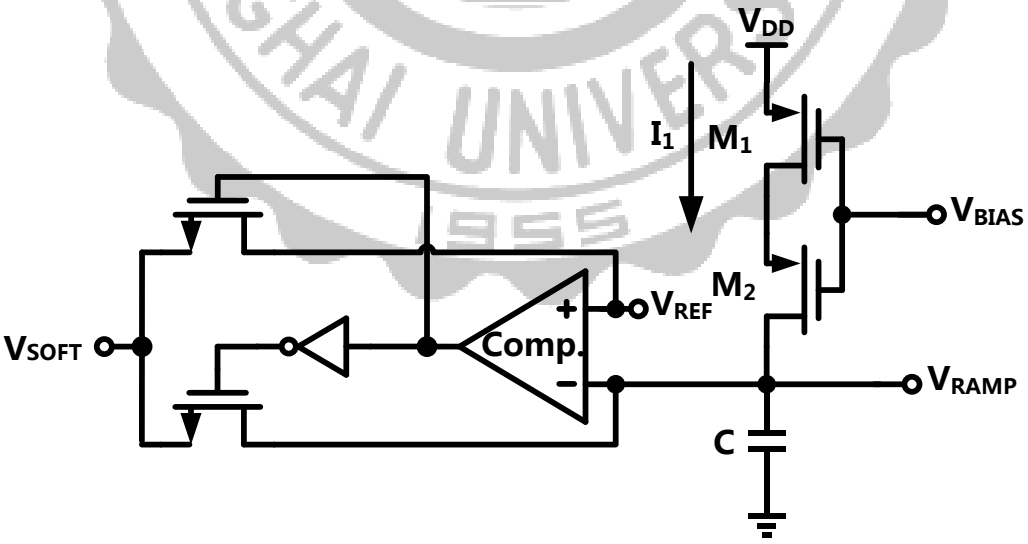


Fig.4.22 Soft-Start Circuit

As the system is powered, the Error Amplifier works not in equilibrium initially and causes duty cycle become immerse that result in inductor produce large current thus may destroy the electronic components on the chip. To avoid instantaneous large current result in damage at electronic components off chip when we introduce the reference voltage to the circuit system, a Soft-start circuit is necessary. Using a Soft-start circuit can make reference voltage rise slow. Here is a capacitor put in the circuit for the purpose to charge I_1 gradually as shown in the Fig4.22. When power is switched on, V_{RAMP} rise slowly through I_1 charges and thus V_{SOFT} will display an upward movement until the V_{RAMP} rises above V_{REF}. The rising slope of V_{RAMP} could be determined by the size of capacitor. Fig.4.23 is the simulation of Soft-start circuit.

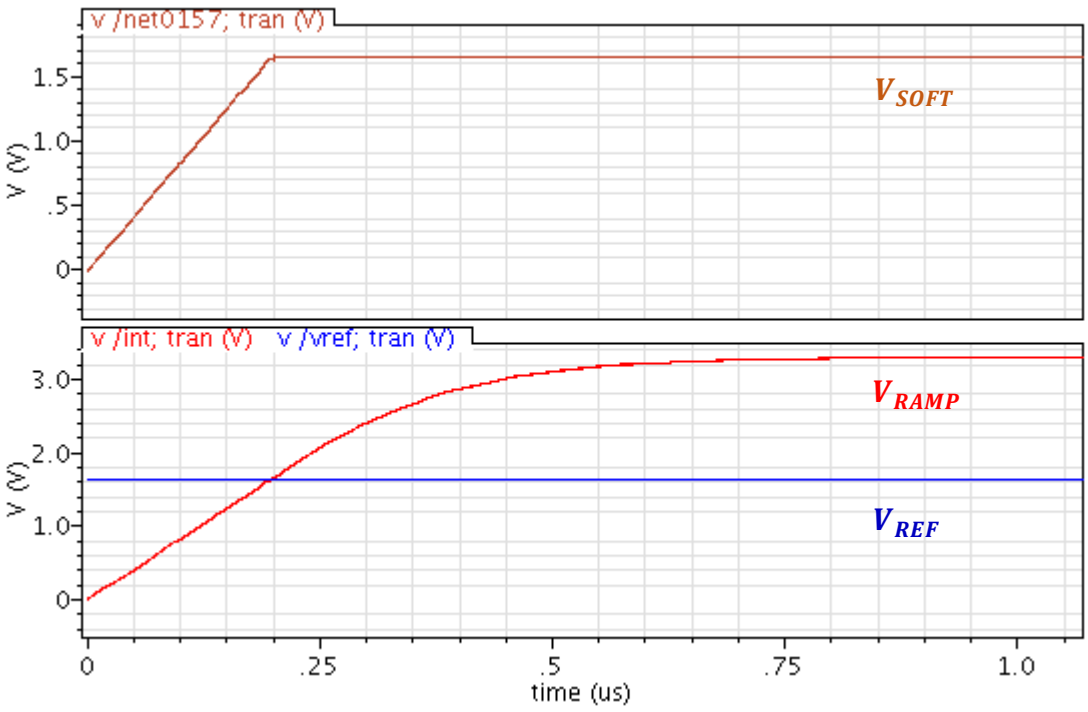


Fig.4.23 Simulation of Soft-Start Circuit

4.3 MULTI-PHASE SPREAD-SPECTRUM CLOCK GENERATOR

(MULTI-PHASE SSCG)

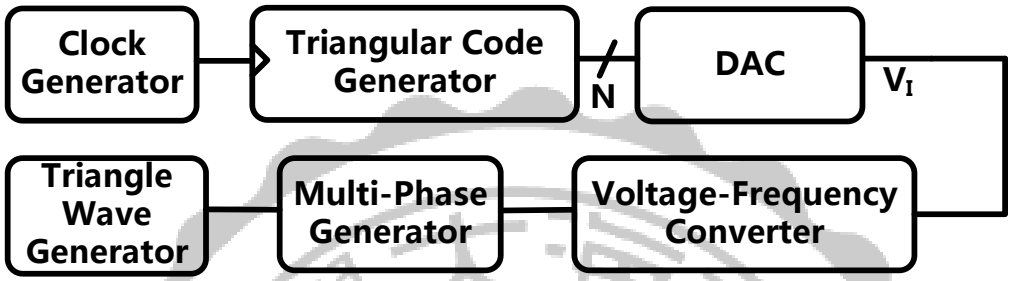


Fig.4.24 Multi-Phase Spread-Spectrum Clock Generator

In Fig.4.24 is depicted for organization of Multi-Phase Spread-Spectrum Clock Generator. First of all, in order to generate a controlling signal, a Clock Generator which is composed of Voltage to Frequency Converter is added to. Next, a Triangular Code Generator is triggered to produce digital triangular waves to a Digital to Analog Converter. After that, analog triangular waves can make frequency modulation be in progress. Thus, a square wave will be converted to four phases of square waves which the Multi-Phase Generator forms. Last but not least, four phases of square waves transform to four phases of triangular waves with modulated frequency and accomplish the whole Multi-Phase SSCG.

4.3.1 VOLTAGE TO FREQUENCY CONVERTER[18]

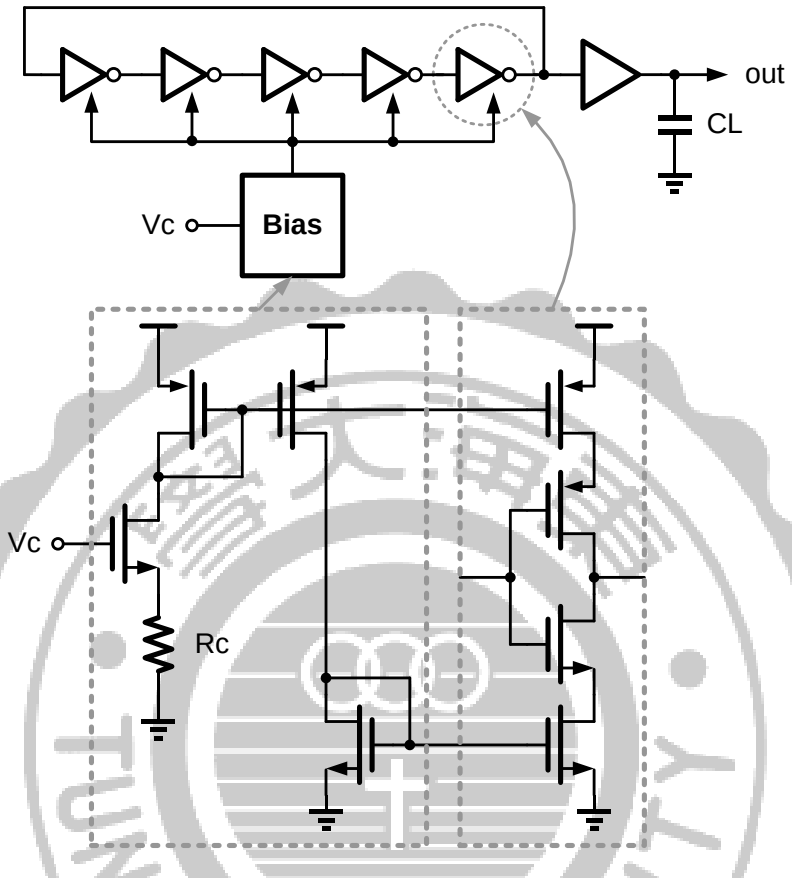


Fig.4.25 Five-staged oscillator

The Voltage to Frequency Converter employs a Current-Starved Ring Oscillator which is composed of five stages of cascaded inverters. Compare with a ring oscillator, the current of inverter is limited by adding current sources controlled through a mirror current as shown in Fig4.25. V_C is able to manipulate oscillated frequency. In this way, as V_C operates at 1.5 V to 1.9 V, the oscillated frequency actuates between 500K to 800K Hz. The advantages of using current-starved ring oscillator are the circuit is simple and easy to design. In addition, it can afford a wider operating frequency

range. The operating frequency depends on numbers of stages of cascaded inverters and time delay T_d.

$$f = 1 / 2 \times T_d \times \mathrm{N}$$

where T_d is related to gate capacitance affecting charging and discharging time resulting in delay.

4.3.2 DIGITAL TRIANGULAR GENERATOR

Digital Triangular Generator is used to control Digital to Analog Converter for the purpose of controlling signals which operate in periodic time. The circuit is composed of Full Adders, D Flip-Flop, and XOR gates as shows in Fig.4.26.

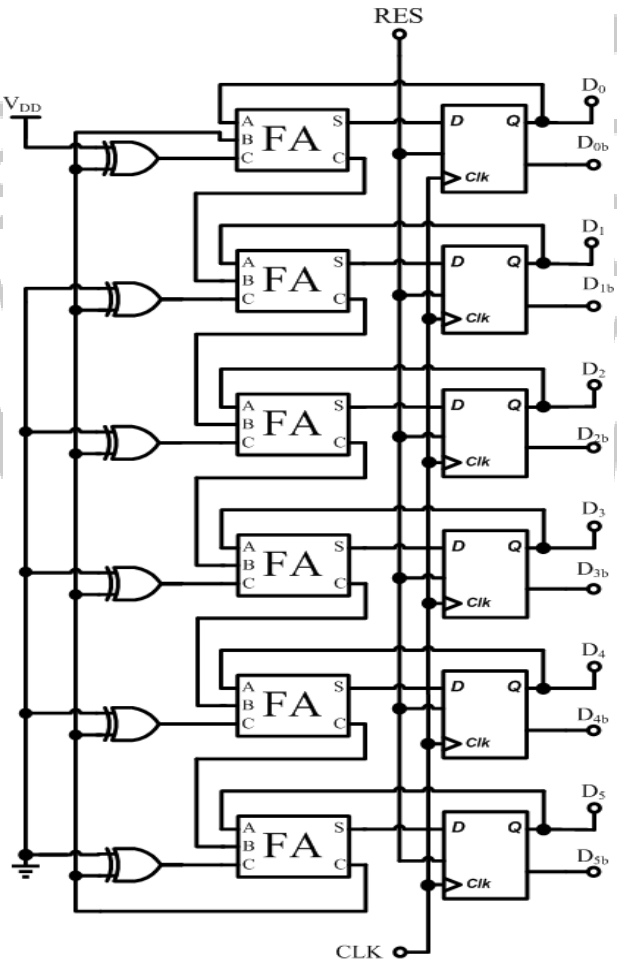


Fig.4.26 Digital Triangular Generator

4.3.3 DIGITAL TO ANALOG CONVERTER[19]

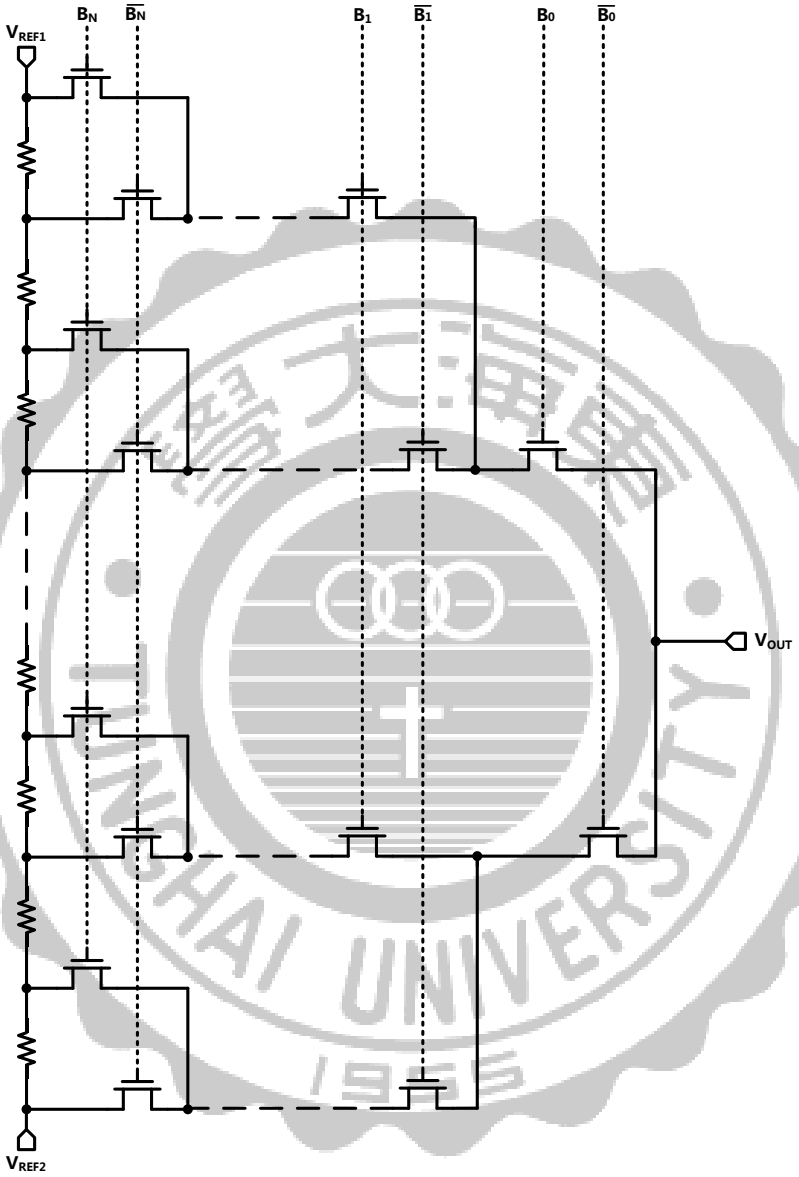


Fig.4.27 Illustration of DAC circuit.

In this work we employ voltage scaling Digital to Analog Converters (DACs). Voltage scaling DACs convert V_{REF} to a set of 2^N voltages which are controlled by a decoder and produce an analog output signal. Voltage

scaling DACs normally uses a series of resistors linked between two reference voltages. For a N-bit converter, there is a string of resistors of $2^N - 1$ illustrated in Fig4.27. We can clearly see that the structure of the voltage scaling DAC is regular relatively and therefore would be proper to implement with MOS technology. Fig.4.28 shows the simulation of DACs. In this work we design the manipulating voltage from1.5V to 1.9V for controlling frequency from 500K to 800K which the next stage VCO is triggered to generate.

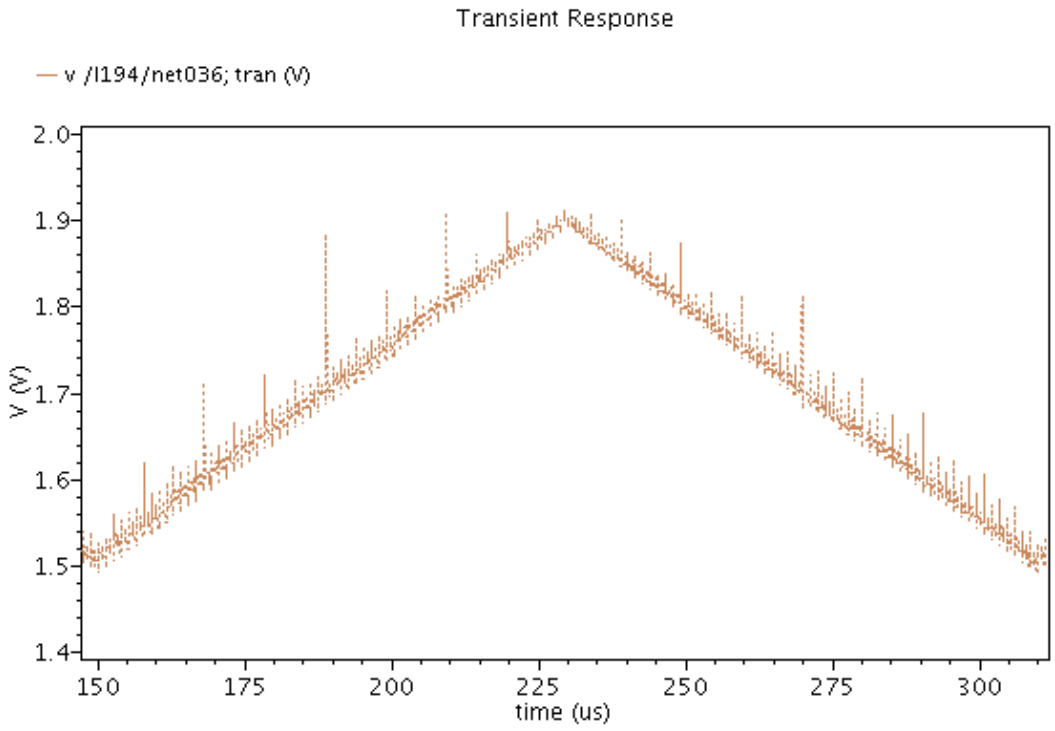


Fig.4.28 Simulation DAC manipulating voltage from 1.5V to 1.9V.

4.3.4 MULTI-PHASE GENERATOR

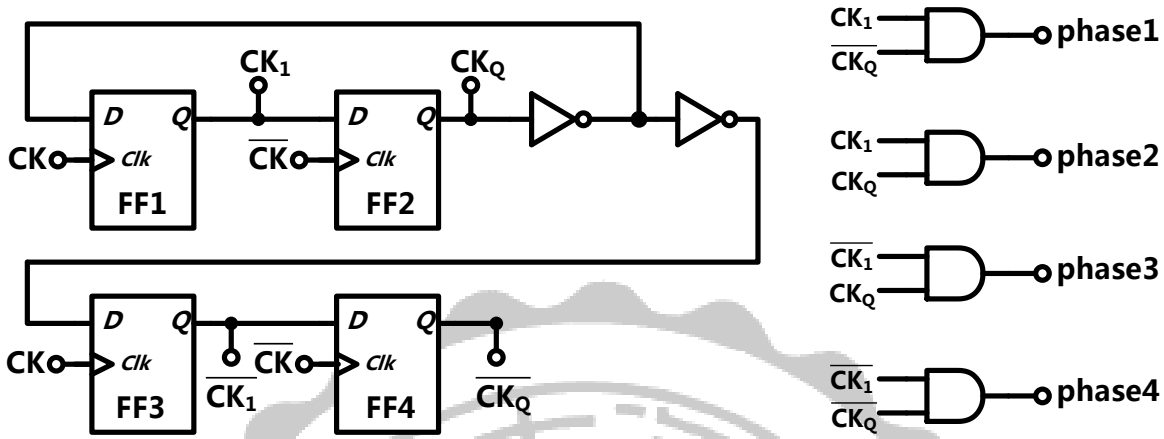


Fig.4.29 Schematic of Multi-Phase Generator

A Multi-Phase generator is employed to generate four quadrature phases. This schematic utilizes D flip-flops and AND gates to take advantage of feature of time delay in digital circuits. Two D flip-flops are linked in cascade and are triggered by CK and $\overline{\mathrm{CK}}$, respectively. For the purpose of producing synchronous signal reversed to CK_1 and CK_Q, another D flip-flops FF3 and FF4 are added to carry on the last one. Furthermore, we can obtain CK_1, $\overline{\mathrm{CK}_1}$, CK_Q, $\overline{\mathrm{CK}_Q}$ as shown in Fig.4.30 and then through AND gates four quadrature phases are generated.

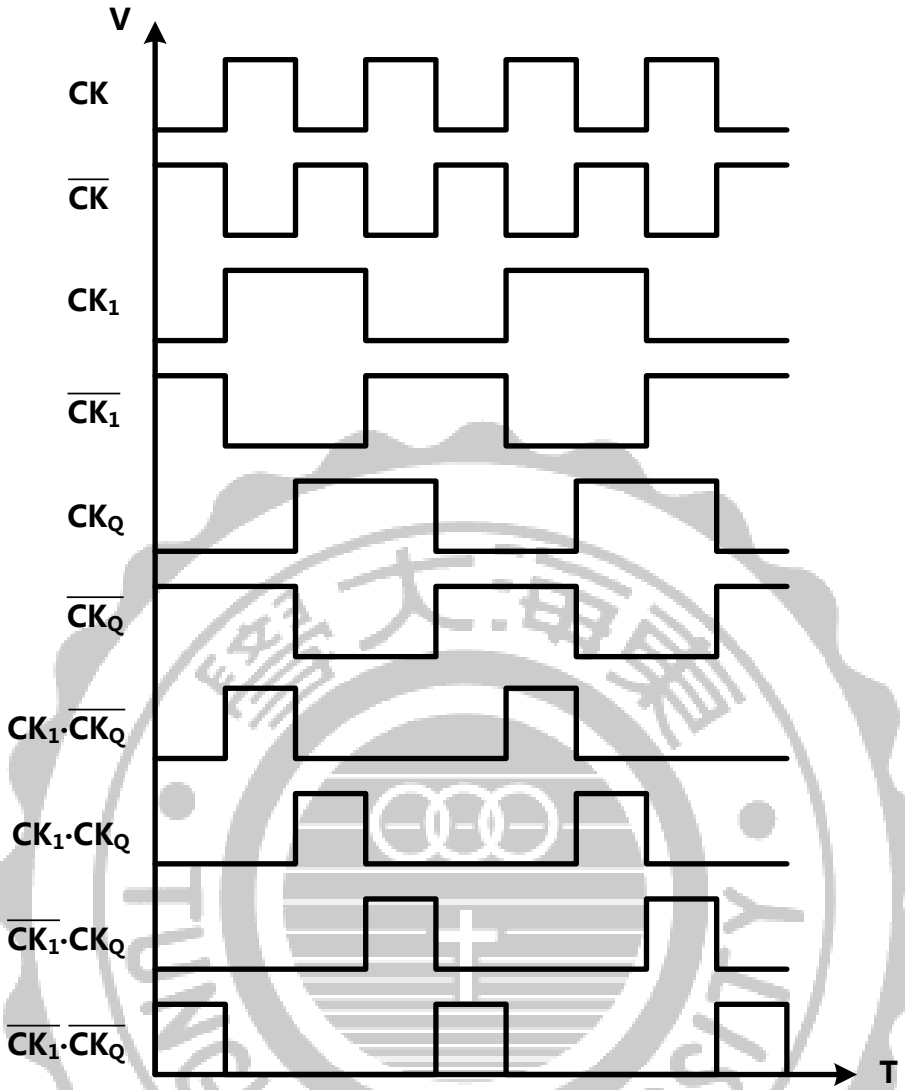


Fig.4.30 A time diagram of the Multi-Phase Generator

4.3.5 QUADRATURE MULTI-PHASE TRIANGULAR WAVE

GENERATOR

The last block, a quadrature multi-phase triangular wave generator, exports four quadrature triangular waves with varied frequency which is manipulated by DAC. Following from the last chains of circuit, by means of feature of the capacitor, the four quadrature square waves would be

transformed to four quadrature triangular waves through it charges and discharges as shown in Fig.4.31.

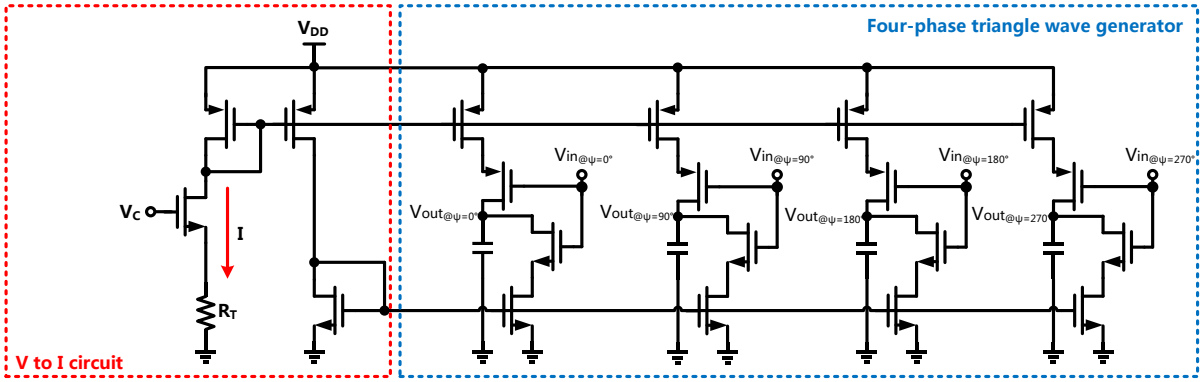


Fig.4.31 Quadrature Multi-Phase Triangular Wave Generator

Fig.4.32 shows the simulation of the designed circuit. Multi-phase generator introduces four square waves to $V_{in@\emptyset=0°}$, $V_{in@\emptyset=90°}$, $V_{in@\emptyset=180°}$, $V_{in@\emptyset=270°}$, respectively. The operating frequency of square waves is controlled by voltage to frequency converter. Then DAC modulates frequency to accomplish effect of EMI reduction.

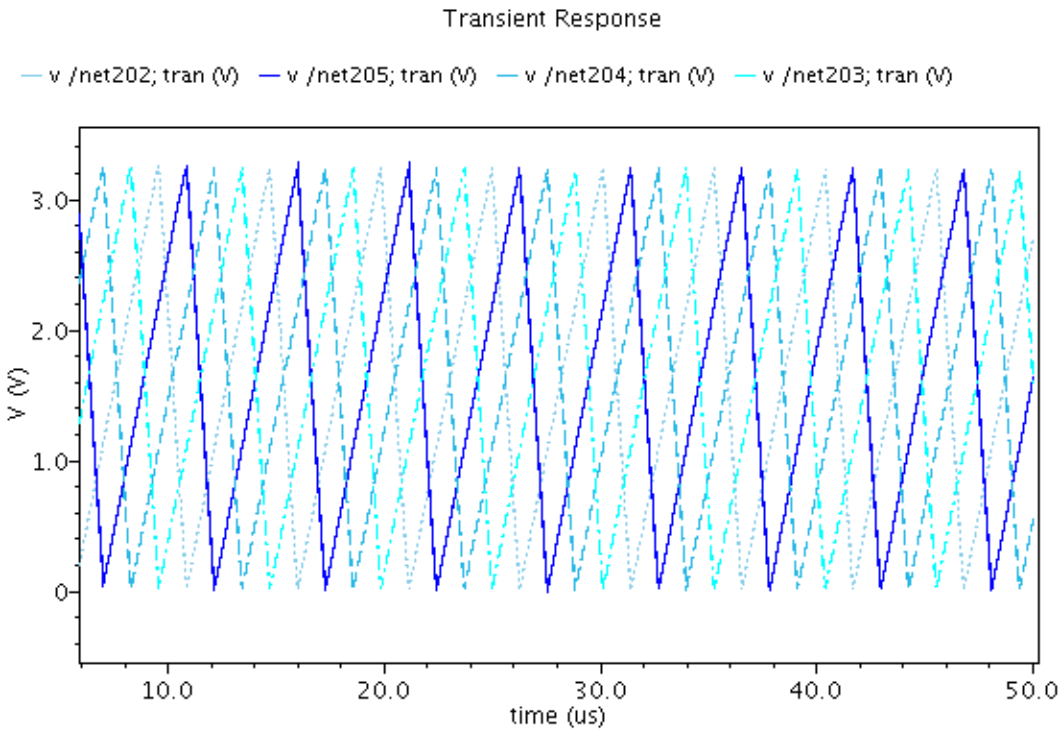


Fig.4.32 Four quadrature phases of Triangular waves

4.4 UNDER VOLTAGE LOCKOUT CIRCUIT (UVLO) CORRESPONDS WITH LDO[20]

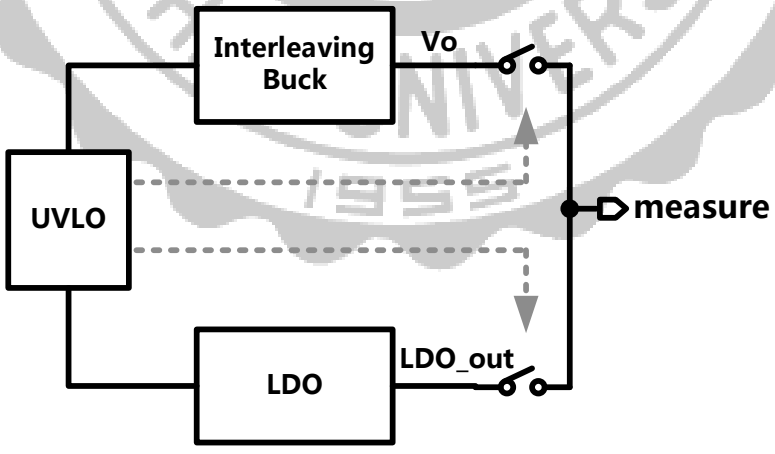


Fig.4.33 UVLO corresponds with LDO and Interleaving Buck

Under Voltage Lockout Circuit can guarantee that system is able to operate without mistakes during the unstable period. That is, as Interleaving Buck is started up, V_O will carry on and in the same time display a climbing linearity for the time being. However, such the situation would cause unnecessary problems for the reason that the Error signal from Error Amplifier is at high voltage at first resulting in the regulator keeping in charge almost. As a result, here are the mechanism named UVLO and LDO which are corresponded into the system in order to solve this problem. An configuration as shown in Fig.4.33 and the illustration as shown in Fig.4.34, the whole system is started up while both regulators begin to operate in the same time. Before Interleaving Buck works in process, LDO supplies the regulated voltage at first. Not until the Interleaving Buck works in stability does the UVLO activate. Thus, UVLO will control two switches that which is chosen to be the output of two regulators. As Interleaving Buck operates in stable, LDO is shut down in the same time the switch linked to LDO is turned off. In the end, the regulated voltage is supplied by Interleaving Buck.

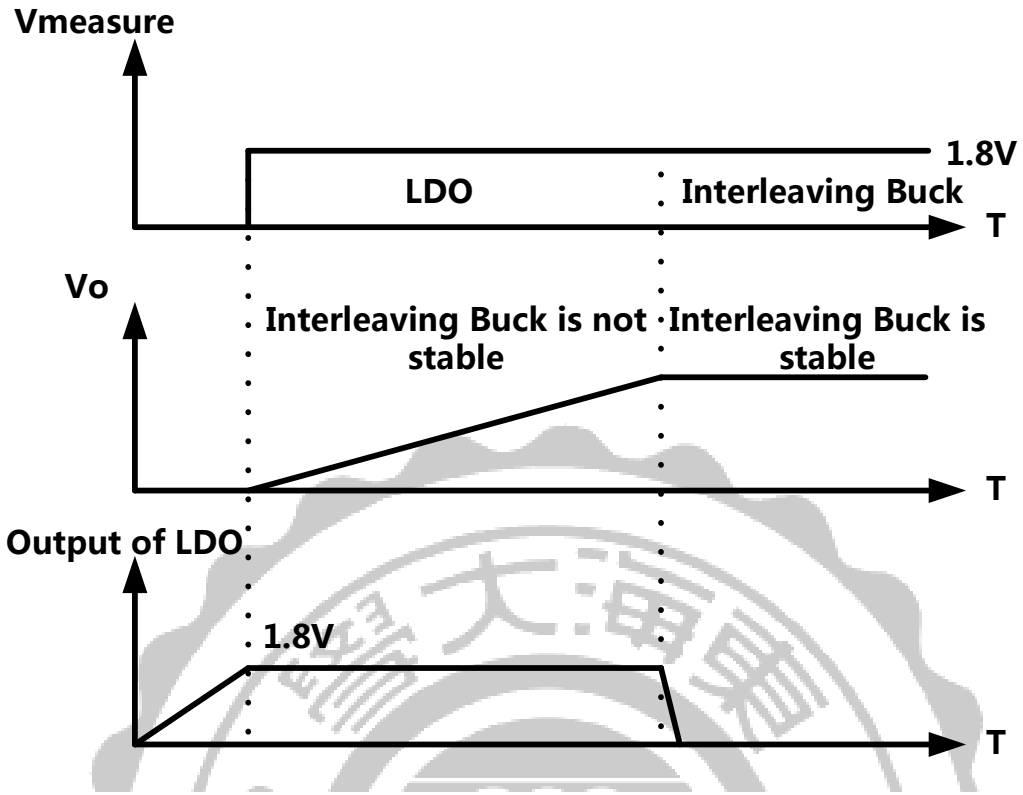


Fig.4.34 illustration of UVLO

4.5 RESULTS OF SIMULATIONS

Fig.4.33 shows the transient response of Buck converter in CCM. We can obviously see that voltage ripple floats significantly. Compare to the Multi-phase SSCG corresponding to Interleaving Quadrature Buck Converter as showed in Fig.4.34, the voltage ripple clearly declines. Fig.4.35 shows that during the load varies in time if the transient response of Buck Converter operates in stability.

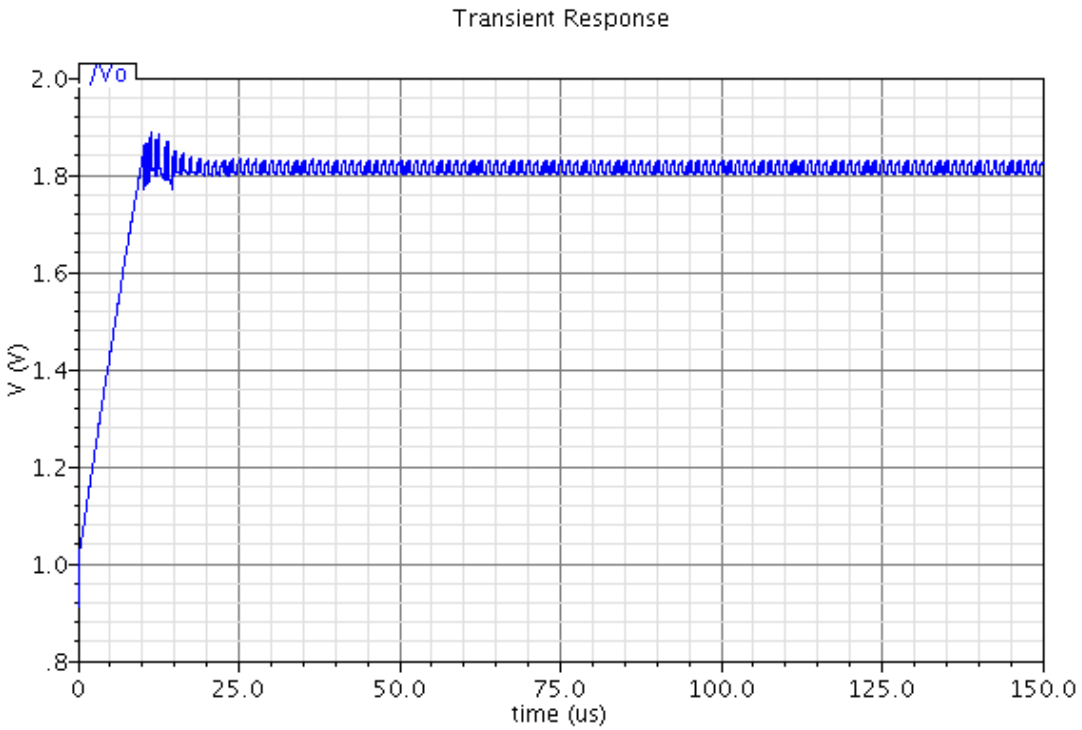


Fig.4.33 Transient response of Buck converter in CCM.

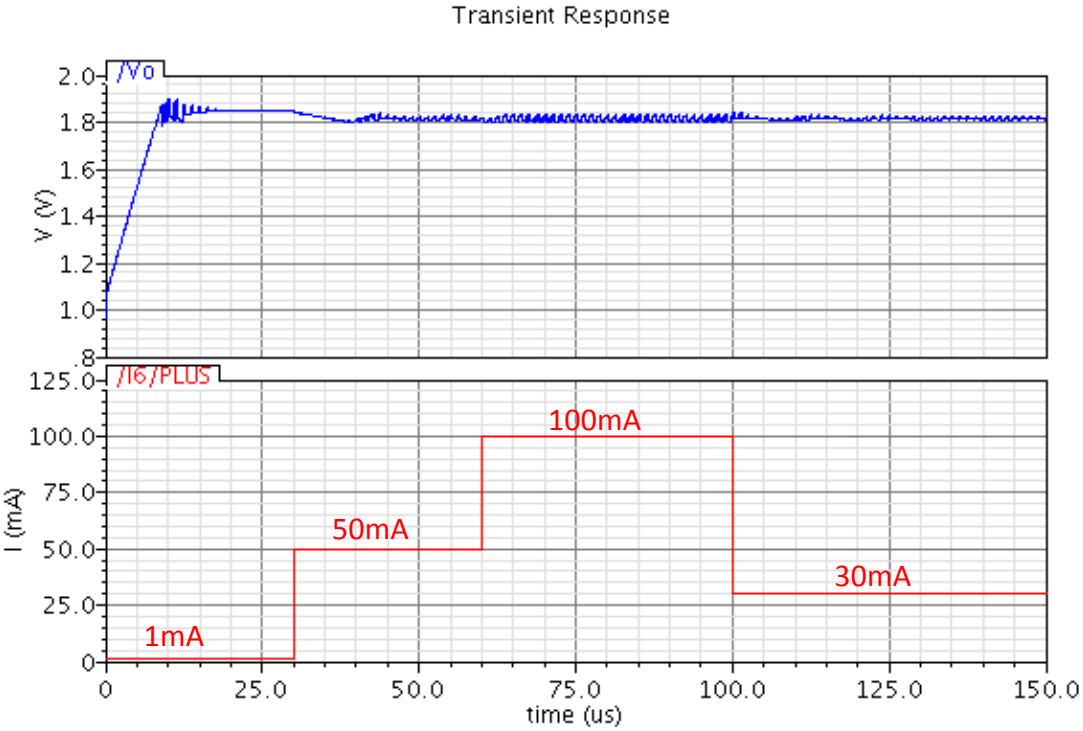


Fig.4.34 Transient response of Buck Converter with load variation.

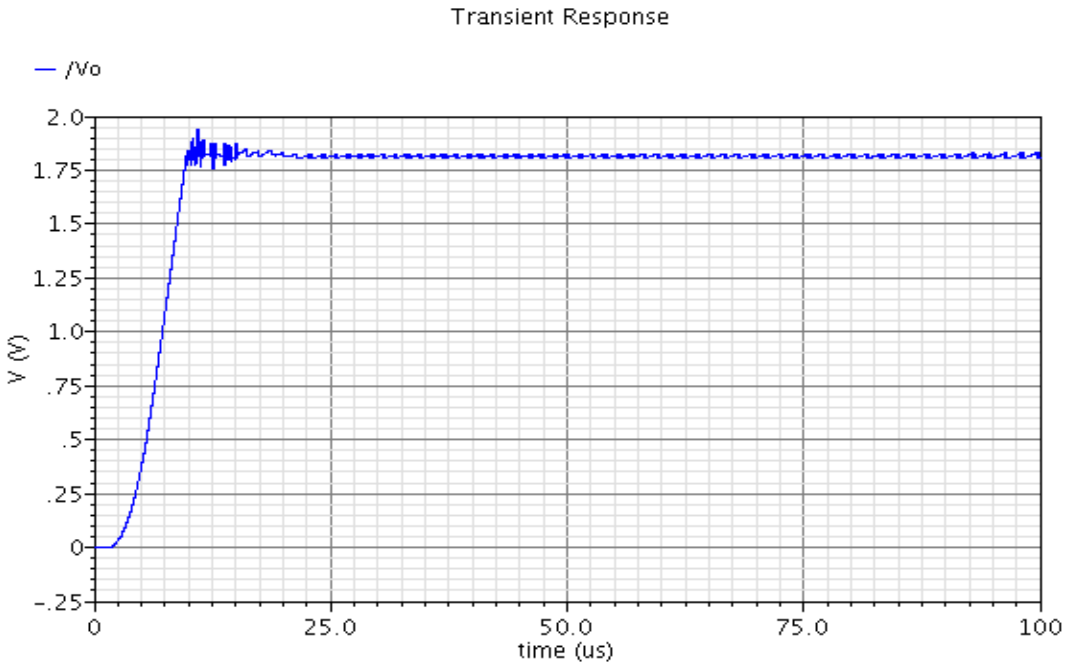


Fig.4.35 Transient response of Interleaving Buck Converter in CCM.

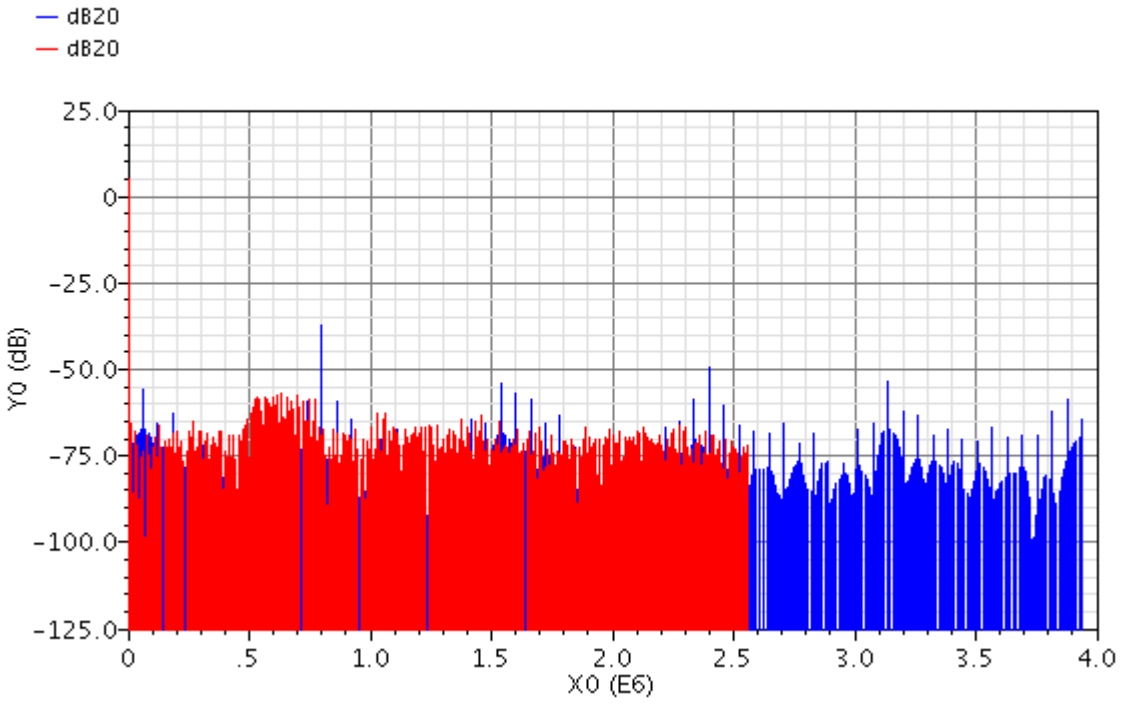


Fig.4.36 Converted spectrum of switching frequency

CHAPTER 5

LAYOUT AND MEASUREMENT

5.1 LAYOUT CONSIDERATION

The proposed Optimized EMI Reduction through Multi-phase Spread-Spectrum Clock Generator Designed for Buck Converter has been integrated in a TSMC 0.18-μm 1P6M 3.3V CMOS Process. Fig. 5.1 shows the microphotograph of the whole chip whose active area occupies 1.14×1.18 mm^2. To prevent POWER MOSFET burnout from huge current at the moment of the system started up, the width of metal connects to POWER MOSFET must be considered. In other words, the wider the width is, the safer the system is. This chip is packaged in a 48-pin IC.

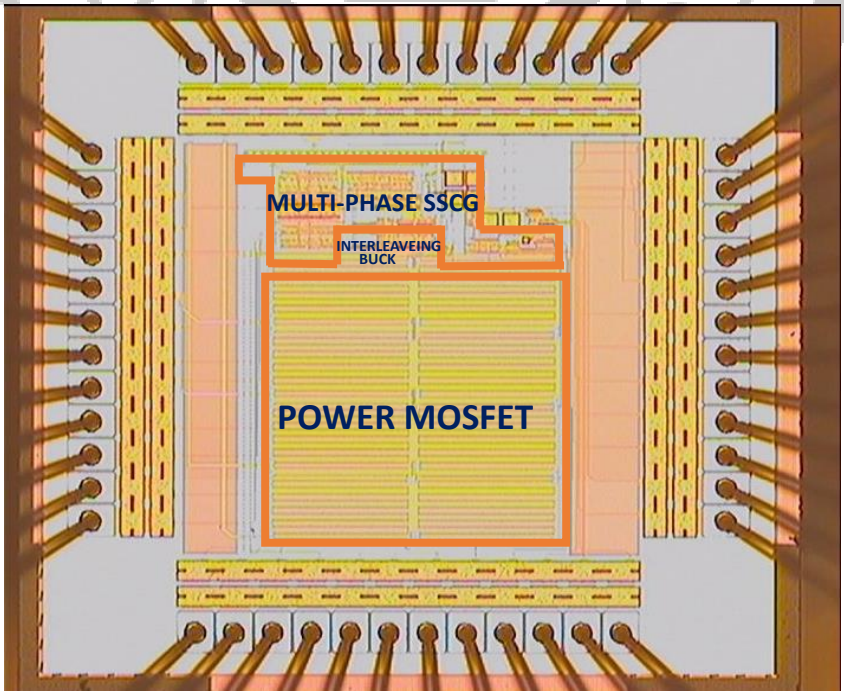
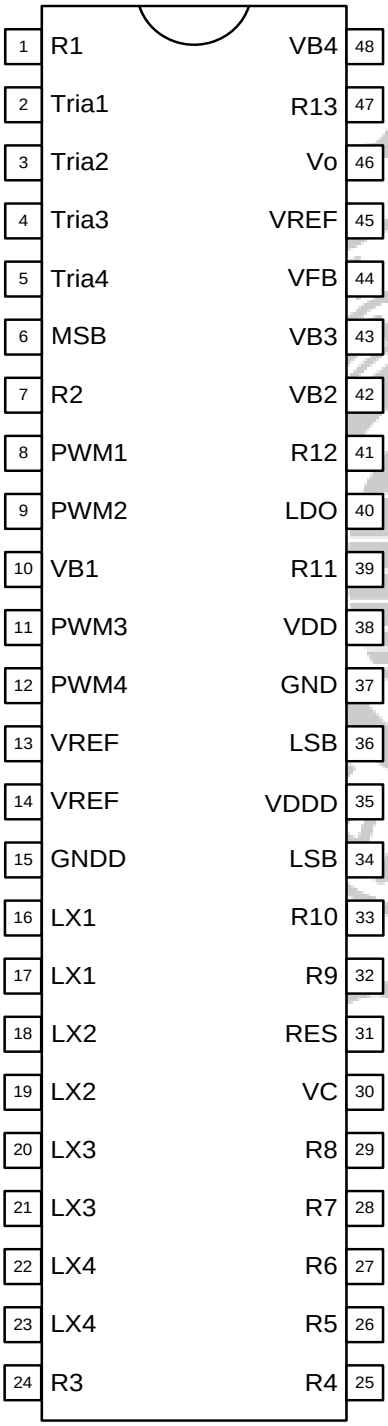


Fig.5.1 Die micrograph of system.

5.2 DATA SHEET

Table.5.1 shows the pin configuration and the pin assignments. The chip is packaged in a 48-pin IC.

Table.5.1 Data Sheet



PIN	NAME	I/O	DESCRIPTION
1	R1	IN	Bias Resistor
2	Tria1	OUT	SSCG Ouput1
3	Tria2	OUT	SSCG Ouput2
4	Tria3	OUT	SSCG Ouput3
5	Tria4	OUT	SSCG Ouput4
6	MSB	IN	DAC MSB Voltage
7	R2	IN	Bias Resistor
8	Tria11	IN	PWM Input1
9	Tria22	IN	PWM Input2
10	VB1	OUT	Bias Output
11	Tria33	IN	PWM Input3
12	Tria44	IN	PWM Input4
13	VREF	IN	Voltage Reference
14	VREF	IN	Voltage Reference
15	GND	-	Analog Ground
16	LX1	OUT	Connect to Inductor1
17	LX1	OUT	Connect to Inductor1
18	LX2	OUT	Connect to Inductor2
19	LX2	OUT	Connect to Inductor2
20	LX3	OUT	Connect to Inductor3
21	LX3	OUT	Connect to Inductor3
22	LX4	OUT	Connect to Inductor4
23	LX4	OUT	Connect to Inductor4
24	R3	OUT	Bias Resistor
25	R4	OUT	Bias Resistor
26	R5	OUT	Bias Resistor
27	R6	OUT	Bias Resistor
28	R7	OUT	Bias Resistor
29	R8	OUT	Bias Resistor
30	VC	IN	Control VCO
31	RES	IN	Control SSCG
32	R9	OUT	Bias Resistor
33	R10	OUT	Bias Resistor
34	LSB	IN	DAC LSB Voltage
35	VDDD	-	Digital power supply
36	Vmeas	OUT	Output of UVLO
37	GND	-	Analog Ground
38	VDD	-	Analog power supply
39	R11	OUT	Bias Resistor
40	LDO	OUT	LDO Output
41	R12	OUT	Bias Resistor
42	VB2	OUT	Bias Output
43	VB3	OUT	Bias Output
44	VFB	IN	Feedback to ERR.
45	VREF	IN	Voltage Reference
46	Vo	OUT	Output of Buck
47	R13	OUT	Bias Resistor
48	VB4	OUT	Bias Output

5.3 TEST SETUP

To setup the environment of measurement, utilization of Power Supply, Spectrum Analyzer, DC Electronic Load, Waveform Generator and Oscilloscope are necessary. In this work, DC Power Supply (Agilent 6621A) is powered to the chip. The inductors and the capacitor are passive elements whose values are 10μH and 10μF respectively linked to the pin of Vout1. The measurement of load regulation employs DC Electronic Load (Prodigit 3310c) cooperated with Waveform Generator (Agilent 33250A) and a Power Switch generating square waves with 1KHz for the purpose of regulating load variation. On Oscilloscope (Tektronix TDS3034B) can observe the conclusion. To measure EMI reduction, we use Spectrum Analyzer (Agilent E4440A) to transfer time domain of V_o into frequency domain.

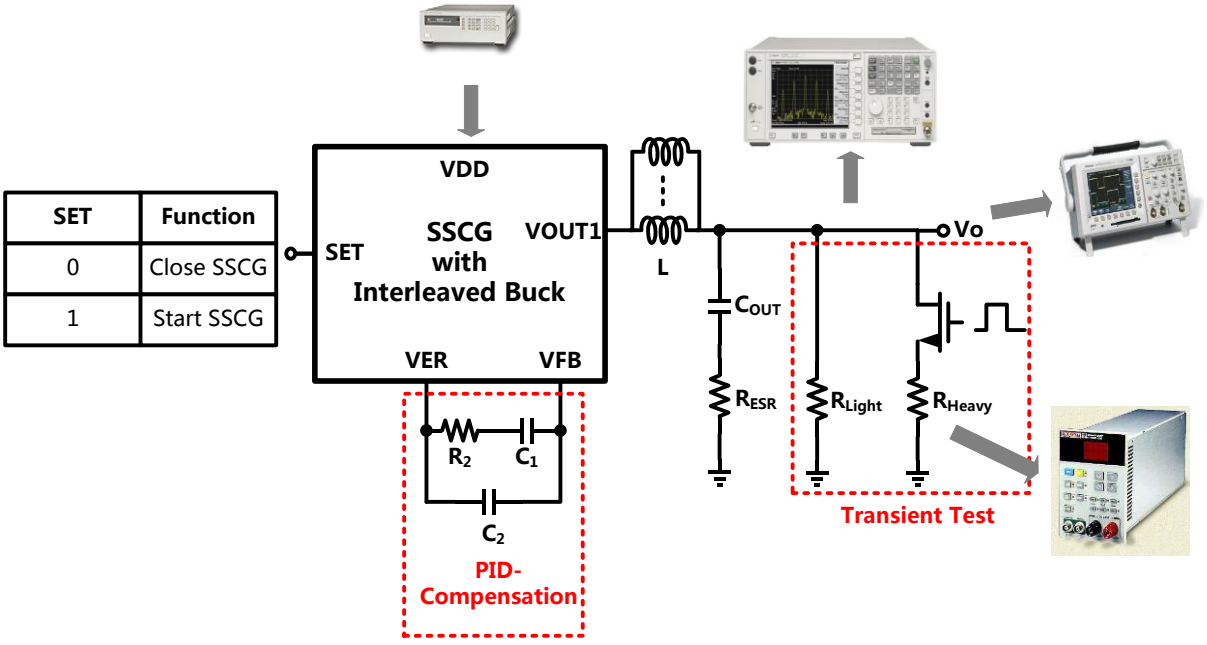


Fig.5.2 Test setup

Here are three parts which separate to measure in the system. The compared EMI reduction between SSCG is active or not is the point we would like to concentrate on. First, we have to assure that when Interleaved Buck operates with switching frequency at 800kHz (in the meanwhile SSCG is turned off), during load regulation that if Buck can work in stable. At the time of load regulation, the duty cycle variation and ripple voltage would be observed. In addition, we manipulate switching frequency from 500kHz to 800kHz to test if Buck would operate without mistakes. Second, to compare EMI reduction of Interleaved Buck with SSCG to the one without SSCG, we employ Spectrum Analyzer to analyze V_o of spectra and obtain the difference. As a result, the amount of EMI among Buck, Interleaved Buck and SSCG with Interleaved Buck can be compared with each other, and prove that this chip could reduce more EMI when each mechanism startups.

REFERENCE

[1] S. Jose, “Spread Spectrum Timing for Hard Disk Drive Applications,” pp. 1-3, Feb. 2005.

[2] A. Santolaria, J. Balcells, D. Gonzalez, J. Gago, and S. D. Gil, “EMI reduction in switched power converters by means of spread spectrum modulation techniques,” presented at the 2004 IEEE 35th Annual Power Electronics Specialists Conference (IEEE Cat. No.04CH37551, 2004, vol. 1, pp. 292–296 Vol.1.

[3] M.-L. Yeh, W.-R. Liou, H.-P. Hsieh, and Y.-J. Lin, “An Electromagnetic Interference (EMI) Reduced High-Efficiency Switching Power Amplifier,” *IEEE Trans. Power Electron.*, vol. 25, no. 3, pp. 710–718, 2010.

[4] K. B. Hardin, J. T. Fessler, and D. R. Bush, “Spread spectrum clock generation for the reduction of radiated emissions,” presented at the Proceedings of IEEE Symposium on Electromagnetic Compatibility, 1994, pp. 227–231.

[5] A. Santolaria, J. Balcells, D. Gonzalez, and J. Gago, “Evaluation of switching frequency modulation in EMI emissions reduction applied to power converters,” presented at the IECON'03. 29th Annual Conference of the IEEE Industrial Electronics Society (IEEE Cat. No.03CH37468), vol. 3, pp. 2306–2311.

[6] A. Knitter, J. Luszcz, and P. J. Chrzan, “Conducted emi mitigation in switched mode dc-dc converters by spread spectrum techniques,” presented at the IEEE Compatibility in Power Electronics, 2005., 2005, pp. 166–171.

[7] H.-I. Pan, C.-H. Cheng, and C.-L. Chen, “A CMOS low dropout regulator stable with any load capacitor,” presented at the 2004 IEEE Region 10 Conference TENCON 2004., 2004, vol. D, pp. 266–269 Vol. 4.

[8] J. C. V. Carlos Eldio Azevedo and P. Santos, “Fully Integrated DC-DC Buck Converter,” pp. 1–10, Apr. 2015.

[9] B. A. Miwa, D. M. Otten, and M. E. Schlecht, “High efficiency power factor correction using interleaving techniques,” presented at the Applied Power Electronics Conference and Exposition, 1992. APEC '92. Conference Proceedings 1992., Seventh Annual, 1992, pp. 557–568.

[10] C. Chang and M. A. Knights, “Interleaving technique in distributed power conversion systems,” *IEEE Transactions on Circuits and Systems I:*

Fundamental Theory and Applications, vol. 42, no. 5, pp. 245–251, 1995.

[11] P. Zumel, O. Garcia, J. A. Cobos, and J. Uceda, "Exploring interleaved converters as an EMI reduction technique in power converters," presented at the IEEE 2002 28th Annual Conference of the Industrial Electronics Society. IECON 02, vol. 2, pp. 1219–1224.

[12] B. A. MiwaMassachusetts Institute of Technology. Department of Electrical Engineering and Computer Science, *Interleaved Conversion Techniques for High Density Power Supplies*. 1992.

[13] J. Mon, J. Gago, D. Gonzalez, J. Balcells, R. Fernandez, and I. Gil, "A new switching frequency modulation scheme for EMI reduction in multiconverter topology," presented at the 2009 13th European Conference on Power Electronics and Applications, 2009, pp. 1–8.

[14] R. Gregorian, *Introduction to CMOS OP-AMPs and comparators*. Wiley-Interscience, 1999.

[15] C. Yoo, "A CMOS buffer without short-circuit power consumption," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 47, no. 9, pp. 935–937, 2000.

[16] L.-W. Hu, "***Design of Fast Transient Response Buck Converter using Pulse Width Modulation***
," pp. 1–64, Aug. 2014.

[17] S. W. H. L. L. C. S. F. L. G. Yuan Gao, "A Novel Zero-Current-Detector for DCM Operation in Synchronous Converter," pp. 1–6, May 2012.

[18] H. Liu, X. Zhang, Y. Dai, Y. Lu, and B. Wei, "A wide range low power CMOS radio frequency ring oscillator," presented at the 2009 4th IEEE Conference on Industrial Electronics and Applications, 2009, pp. 1340–1344.

[19] "Allen, Holberg - CMOS Analog Circuit Design second edition," pp. 1–794, Dec. 2009.

[20] S.-R. Wu, "**DC to DC IC Design for Driver System of Ultra-High Performance Lamp** ," pp. 1–157, Jul. 2007.