東海大學電機工程學系

碩士論文

以邊界條件調節電場的高壓 SOI 元件

The Boundary Condition Adjusted Electric Field Distribution in Smart-cut SOI for High Voltage Applications

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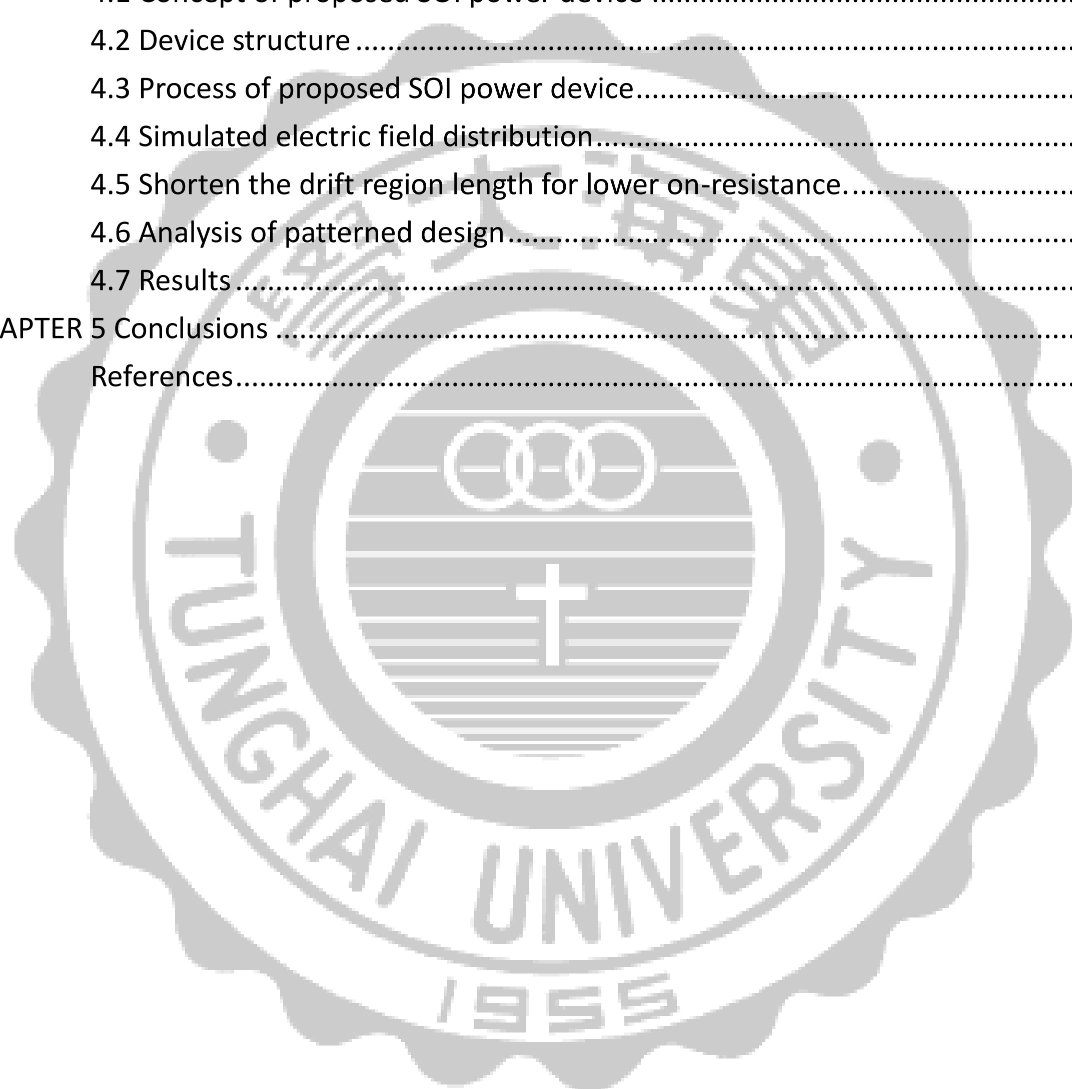

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Abstract

The purpose of this thesis is to adjust and unify the surface electric field of silicon-on-insulator (SOI) power devices by using a low dielectric constant buried material, in which air and SiO_2 are alternately placed. The proposed device is compared with conventional SOI and buried air gap structure (BAGS) SOI devices**.** The breakdown voltage of the proposed structure is higher than the BAGS SOI devices which has half air in the buried oxide layer.

The main consideration of the device design is all in the insulator mask that defines: the air position, air width, and segment quantity. TCAD simulation is used to find out device properties. The optimized device with the proposed structure has shorter drift region length, smaller $R_{on,\,sp}$, and can still keep the breakdown voltage higher than 600V.

CHAPTER 1 Introduction

1.1 The background

Superior isolation is very important for power integrated circuit (PIC), as low-voltage and high-voltage devices are put together on the same chip. [1] The isolation technique of the power integrated circuit adds protection for the leakage current. [2]The isolation processes used in the manufacture of integrated circuits are incorporated to keep the individual components within each monolithic chip from interacting with each other, [3] i.e. isolation from one another. Several different techniques have been developed to accomplish this function. These are: Self isolation, Junction isolation, and Dielectric isolation. [4]The self isolation technique can be applied when single devices inherently form reverse-biased junctions. Processing of this isolation type is very simple since no special steps have to be introduced, e.g. LOCOS and trench isolation. [5] A disadvantage of this technique is the high number of parasitic devices generated due to the missing isolation, and the flexibility of the circuit is reduced. [6] In the junction isolation technique, additional doped areas are introduced between devices to ensure proper isolation. For p-type

substrates with n-type epitaxial layers, diffused p-regions from the surface down to the substrate are used. [7] This technique is still cost efficient and is often used since it gives higher flexibility than the self isolation technique. From the isolation's point of view, the best option is the dielectric isolation. [8] Here, a silicon dioxide layer separates the devices leading to much lower ohmic and capacitive coupling compared to junction isolation techniques. There are no parasitic effects between the transistors, since there are no additional pn-junctions. In addition, high-voltage silicon-on-insulator (SOI) devices exhibit lower on-resistance than junction isolation devices when used in high-side switching applications. [9] SOI can provide ideal dielectric isolation, so they become very promising for PIC applications. [10]

1.2 Motivation

The breakdown voltage of SOI device is limited by the vertical electric field. [11] The low breakdown voltage restricts its application in power and high voltage ICs. To address the issue, the ultra-thin SOI structures have been proposed. [12][13] But as silicon film thickness is reduced, series resistance of SOI devices increases. Silicide technology, which is used to reduce resistance in SOI, is difficult to apply to ultra-thin SOI wafer. Due to the cost and yield

rate, we don't consider to increase the thickness of epitaxial and buried oxide layer to increase the breakdown voltage. It is well known to the device engineers that linearly graded doping that is heavy to light from cathode to anode will result in a more uniform electric field. [14]~[18] But this ideal technique is difficult to achieve in the practical application. A new structure that can achieve uniform electric field is proposed in this thesis. An effective technique for enhancing breakdown voltage is to increase the electric field in the epitaxial layer, yet without increasing the critical field of the entire device. Above-mentioned concept was demonstrated in the Buried Air Gap Structure (BAGS) device. [19][20] Because both of the two structures are made of air and SiO_2, the BAGS device is compared with the proposed structure in this thesis.

CHAPTER 2 Literature review

2.1 Literature review of SOI-Process

2-1-1 BESOI (Bonding & Etch back)

First, prepare two silicon wafers, the device wafer and the handle wafer. Second, epitaxs the device wafer to become the etch stop layer, and to grow the oxide layer in handle wafer by high temperature to make a lower defect. After bonding with the Vender Walls force, strengthen the links of the two wafers by thermal annealing, and polished by CMP as shown in Fig.1. [21]

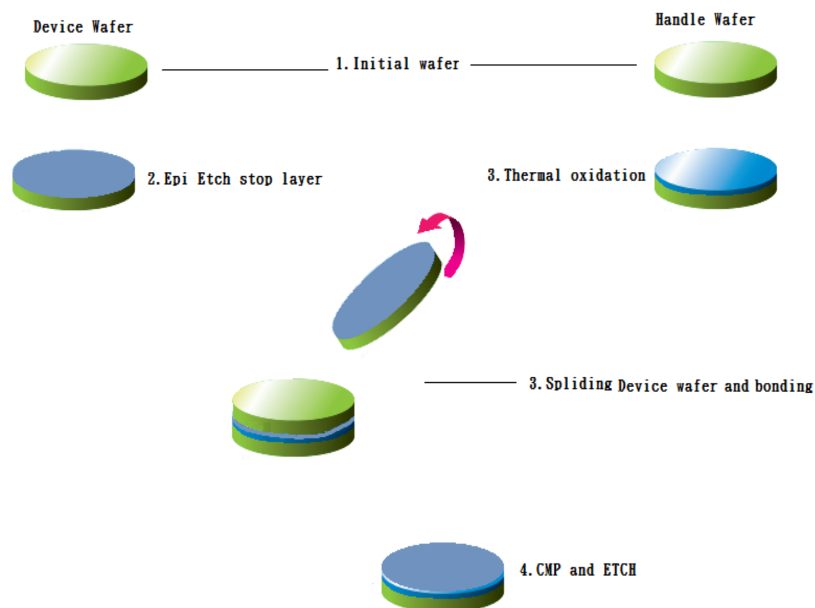

Fig.1 BESOI Process

2-1-2 SDB (Silicon direct bonding)

Two silicon wafers were oxidized, the surface was closed to each other by Vander Waals force after hydrophilic process. Because the bonding is not solid at room temperature, it needs annealing for reinforce. After the bonding, the thickness is thinned to reach a desired thickness.

Buried oxide layer thickness is set by thermal oxidation time and temperature, so the quality of the silicon layer and the buried oxide layer is better.

SDB is easy to get thicker SOI, but limited thinning technique is not easy to get thin epitaxial layer. It is shown in Fig.2. [22]

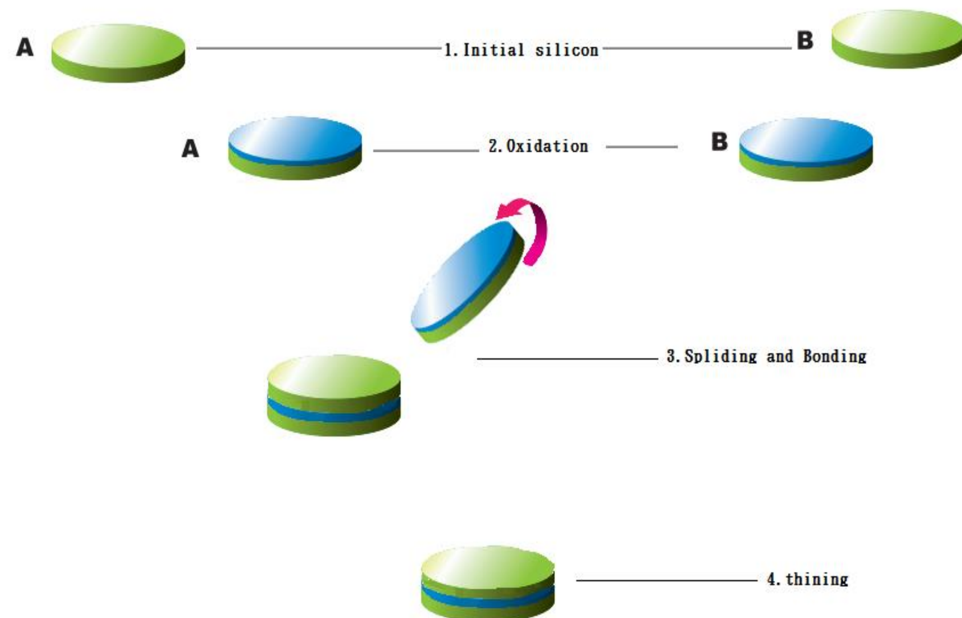

Fig.2 SDB Process

2-1-3 ELTRAN (Epitaxial layer transfer)

The CVD Si epitaxial is growth on porous Si, bonding, and selective etching in conjunction with the novel phenomena by hydrogen annealing to flatten the rough etched surface in no expense of Si. The last established technique is highly reproducible splitting in the porous Si layer and reuse the seed wafer several times. Water jet is injected at the edge of bonded pair and splits entirely the two wafers within the thin porous Si layer. The porous Si layer has the stress concentrated double layered structure, resulting the both split wafers (SOI and seed Wafer) covered by the porous Si protective layers.

The process is shown in Fig.3. [23], [24]

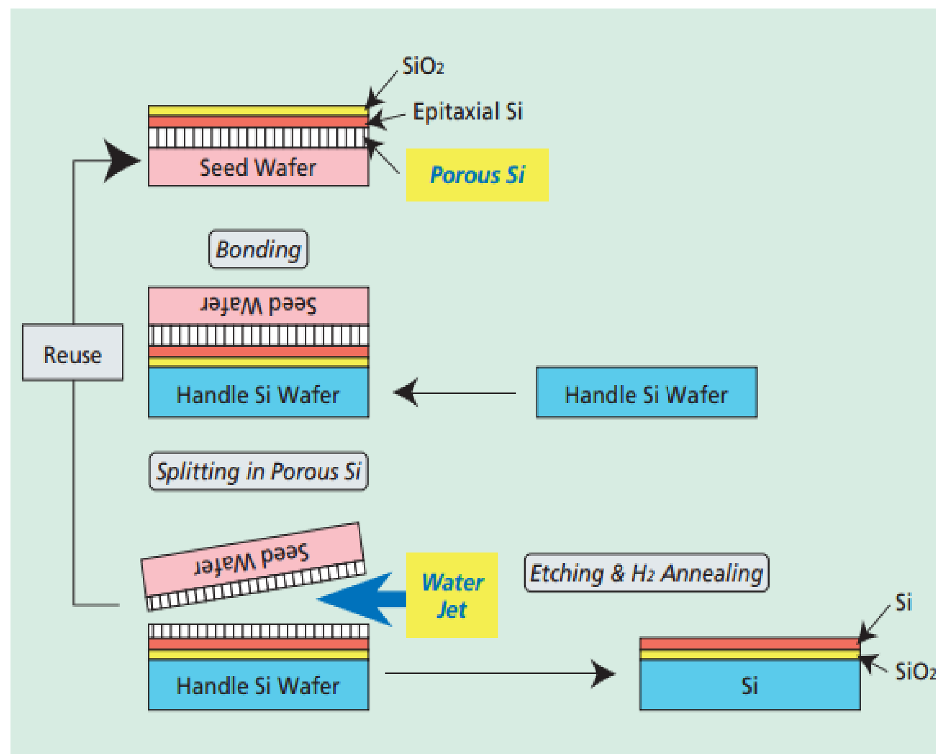

Fig.3 ELTRAN Process[24]

2-1-4 SIMOX (Separation by IMplanted OXygen)

First, to implant a large number of oxygen ions below the surface of a silicon wafer. The silicon wafer is then to anneal to get a uniform buried SiO_2 layer with distinct interfaces with the two adjacent silicon layers and also to eliminate lattice defects, finally polished by CMP.

The process is shown in Fig.4. [25], [26]

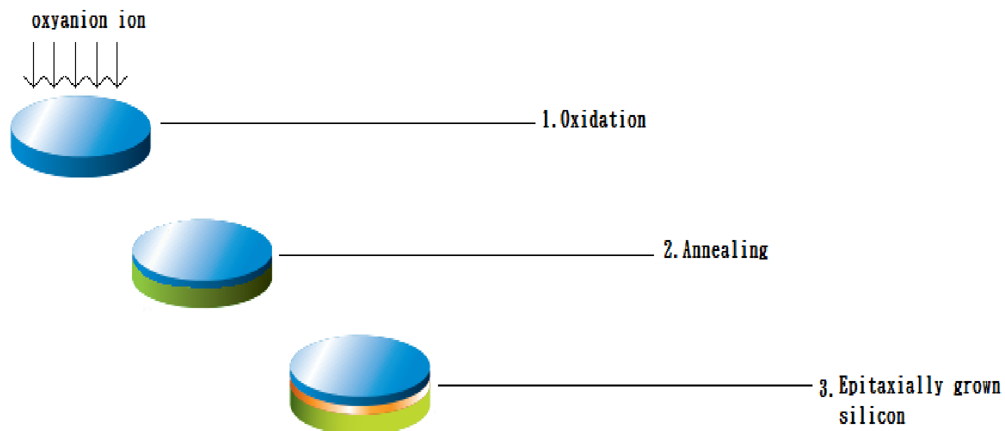

Fig.4 SIMOX Process

2-1-5 Smart-Cut [27]

First, oxidation on one piece of wafer or two pieces of wafers, and then one of thermally oxidized wafer is implanted with a high dose of hydrogen. Flip and bond the handle wafer then to annealing. The area of high doping of H^+ will break before the annealing, finally polish the wafer by CMP and the remaining wafers can be reused. The process is shown in Fig.5.

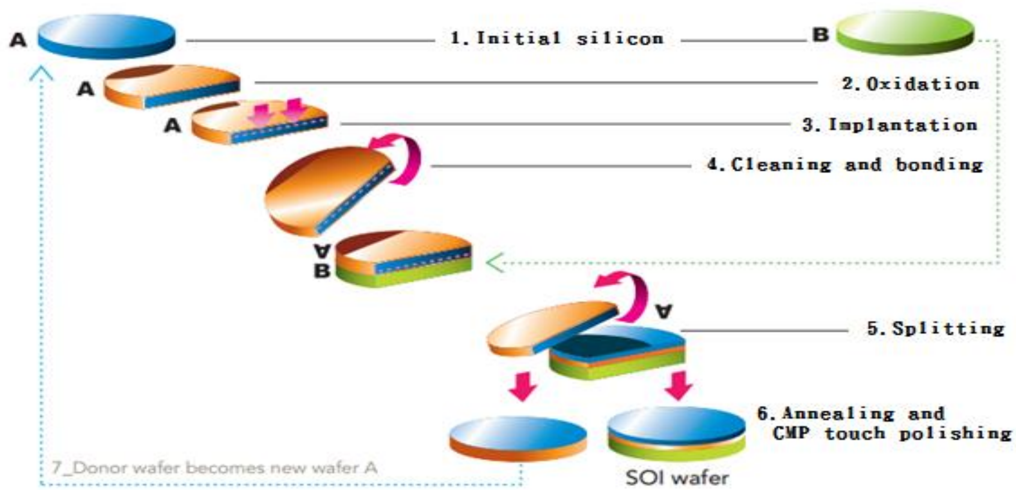

Fig.5 Smart-Cut Process[27]

The application as low-voltage and high-voltage devices are put together on the same chip is an important issue, so we want to develop our device using the smart-cut technology and the wafer of smart-cut can be reused without waste. The size of our device is following the specifications which are provided by SOITEC, Fig. 6. [28]

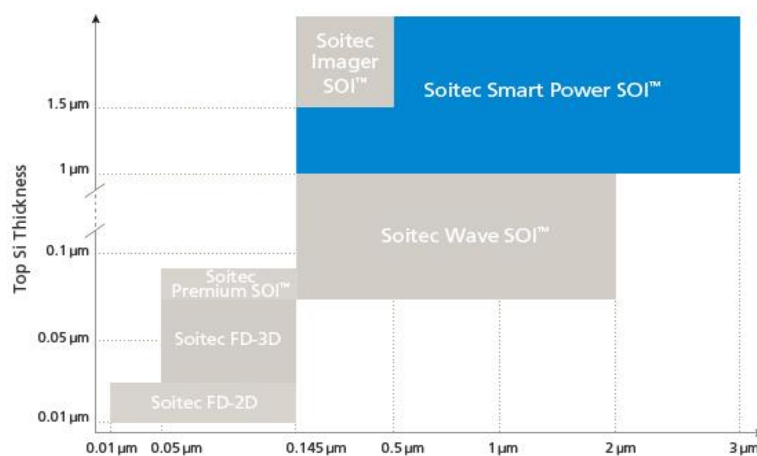

Fig.6 SOITEC offers several product lines to address specific application [28]

2.2 Literature review of SOI power devices

2-2-1 Epitaxial & buried oxide layer thickness

The breakdown voltage of conventional SOI device is limited by epitaxial layer thickness buried oxide layer thickness, [29] and the drift region length. Most of the voltage is supported by the buried oxide layer. The maximum electric field strength at the interface between silicon and the buried oxide is limited by that of the silicon region at the interface. In general, the thickness for both materials are thicker, the breakdown voltage is higher. However, if the epitaxial layer is too thick the buried oxide layer can't share fully the cathode voltage, the breakdown will occur early in the epitaxial layer. The breakdown voltage of thicker buried oxide layer is not in a linear rise, and there have thermal conduction and thermal resistance rising problems. [30][31] If we only use the PN doping to improve the breakdown voltage, there still have problems of the conflict between the on-resistance and breakdown voltage. Basically, the thin SOI structure is the RESURF effect that is based on the electric field distribution in the lateral depletion layer and the buried oxide. With the substrate at the ground potential, the breakdown voltage of SOI can be expressed as: [32]

$$BV = (\frac{t_{soi}}{2} + \frac{\varepsilon_{si}}{\varepsilon_{ox}} t_{ox}) E_c \quad (2\text{-}1)$$

Figure.7 shows SOI RESURF device, t_{OX} is the oxide layer thickness, and t_s is the drift region thickness.

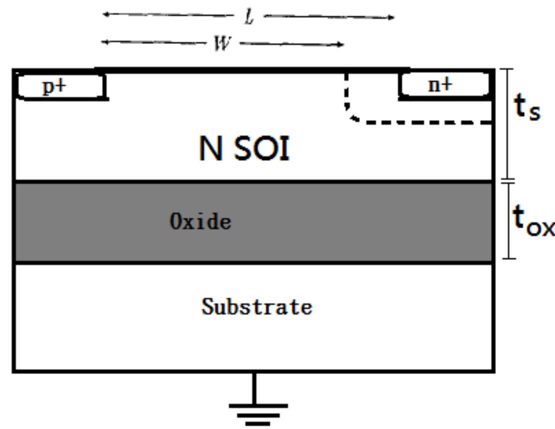

Fig.7 A conventional SOI diode.[29]

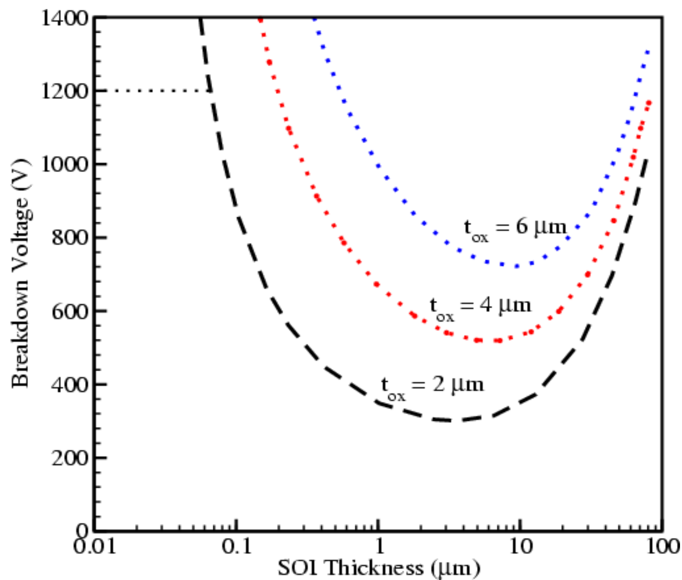

Fig.8 Theoretical BV versus SOI thickness [29]

Figure.8 shows that the theoretical BV versus SOI thickness for three different values of buried oxide thickness, t_{OX}. [29] The BV is increased if the t_s is increased over 3.0um or decreased approximately below 2.0um.

2-2-2 Adjusting the lateral electric field in high voltage devices

2-2-2-1 Linearly doped SOI

According to the RESURF principle [33], the drift region concentration is too high or too low will cause breakdown to occur at drain or source side, respectively. So, an appropriate drift region is also a way to increase breakdown voltage.

Most proposed processes open the mask from drain to source from wide to narrow, and control ion implantation energy and diffusion time to make the drift region produce a linear doping distribution. The illustration of mask and the doping concentration of drift region are shown in Fig.9. [14]~[18]

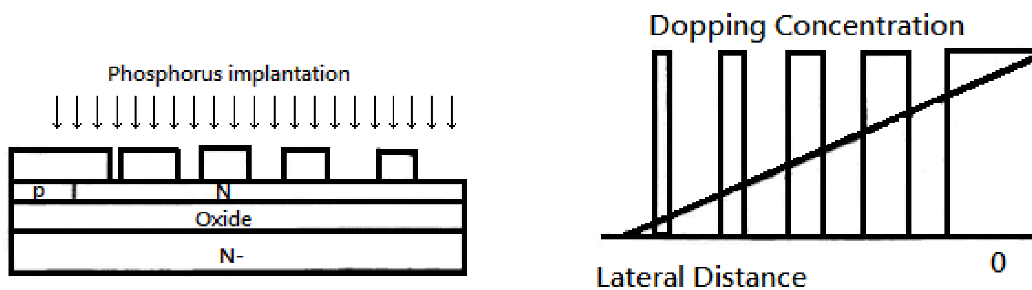

Fig.9 Linearly doped SOI

2-2-2-2 Double RESURF

Double RESURF is a very complicated process of accurate charge control, and requires a well-designed device layout with complete charge balance among all the critical layers. A double RESURF high-voltage P-TOP SOI MOSFET is

shown in Fig.10. [34]

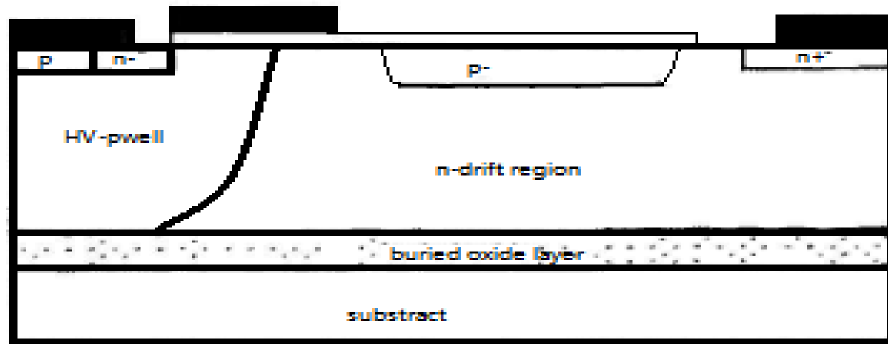

Fig.10 Double RESURF SOI[34]

2-2-2-3 BOSS (Buried oxide Step Structure)

The stepped buried oxide layer make the bottom of drain thicker, the interface of this step generates a new peak to increase the surface electric field. The cross section of the BOSS SOI is shown in Fig.11. [35], [36]

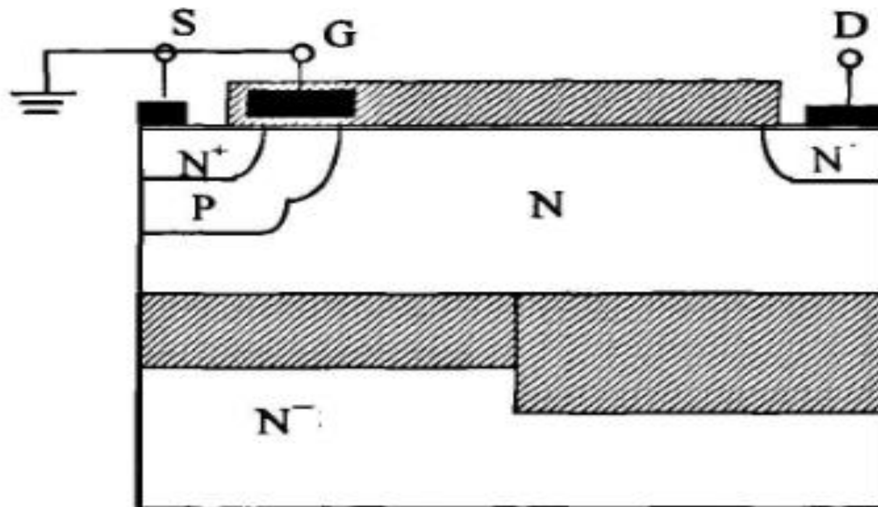

Fig.11 BOSS SOI[35]

2-2-2-4 CamSemi membrane power device

The substrate under the buried oxide layer at the drain to gate side is etched to make the electric potential penetrate through the buried oxide layer and improve the distribution of drift region electric field to increase the pressure effect. The structure is shown inFig.12. [37], [38]

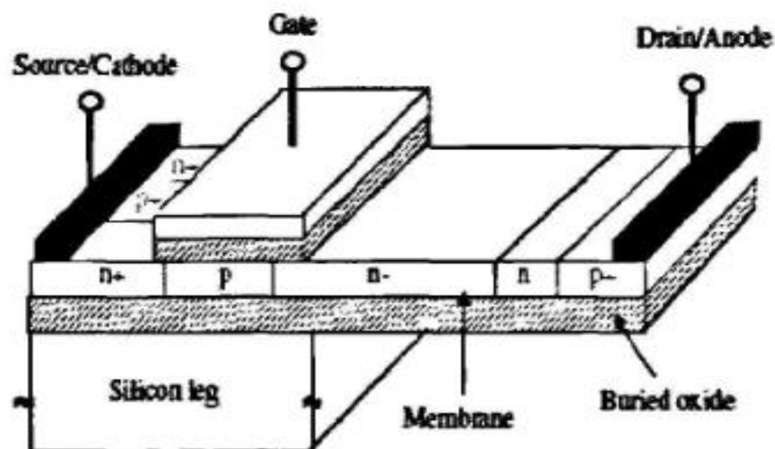

Fig.12 CamSemi membrane power device[37]

2-2-2-5 BAGS (Buried Air Gap Structure)

The buried oxide layer of air and SiO_2 are equally divided as the dielectric layer. The new electric field peak near the middle of drift region pulls down the other peaks within the silicon layer. It is found that the peak electric field near both the source junction and the drain junction are considerably reduced and the breakdown voltage will increase. This structure is shown in Fig.13. [19][20]

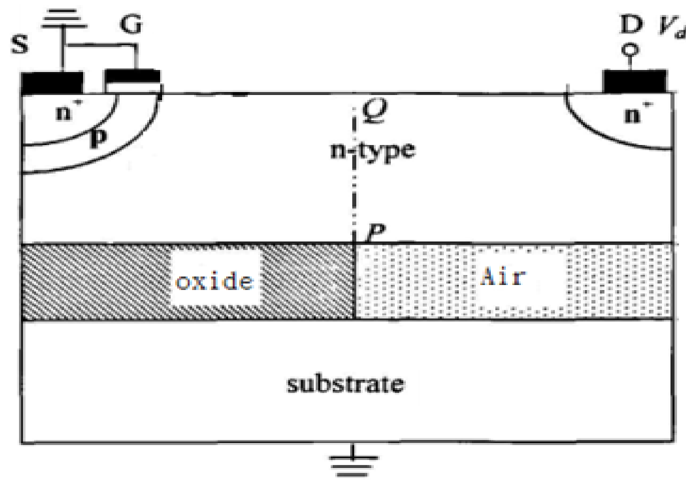

Fig.13 BAGS SOI[19]

2-2-3 Adjusting the vertical electric field in high voltage devices

The substrate of SOI is not like the traditional silicon substrate and as previously mentioned that the epitaxial layer and the buried oxide layer can't be made thick, so, the vertical electric field of the SOI substrate is low. Following are some structures that can enhance the vertical electric field.

2-2-3-1 The ultra thin SOI

From the above 2-2-1, we know that the ultra thin SOI can achieve very high voltage. However, when the thickness is decreased the on-resistance will be increased, so, it's not our choice for power SOI. We can refer to the curve between thickness and breakdown voltage given in Fig. 8. [12][13]

2-2-3-2 The n-type buffered SOI

The n-type buffered SOI using a structure consisting of an n-diffusion layer over 15-μm thick high resistivity n-silicon layer with a 3-μm silicon dioxide. One way to do this is to form a positive charge layer at the interface between the thin silicon layer and the bottom oxide, where shallow n-type diffusion layers are formed directly on the bottom oxide. An appropriate impurity dose in the bottom n-type shallow diffusion layer improves the breakdown voltage. This structure is shown in Fig.14. [39]

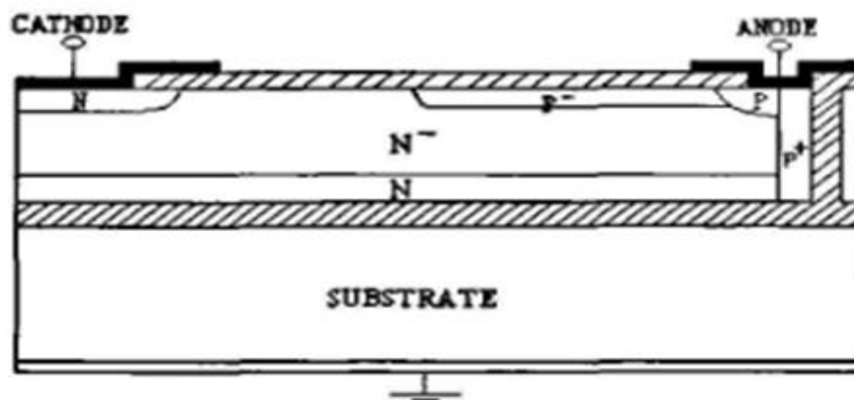

Fig.14 The n-type buffered SOI[39]

2-2-3-3 Buried oxide double-step SOI

The buried oxide has double steps that can collect charges to enhance the vertical electric field. This structure is shown in Fig.15. [40], [41]

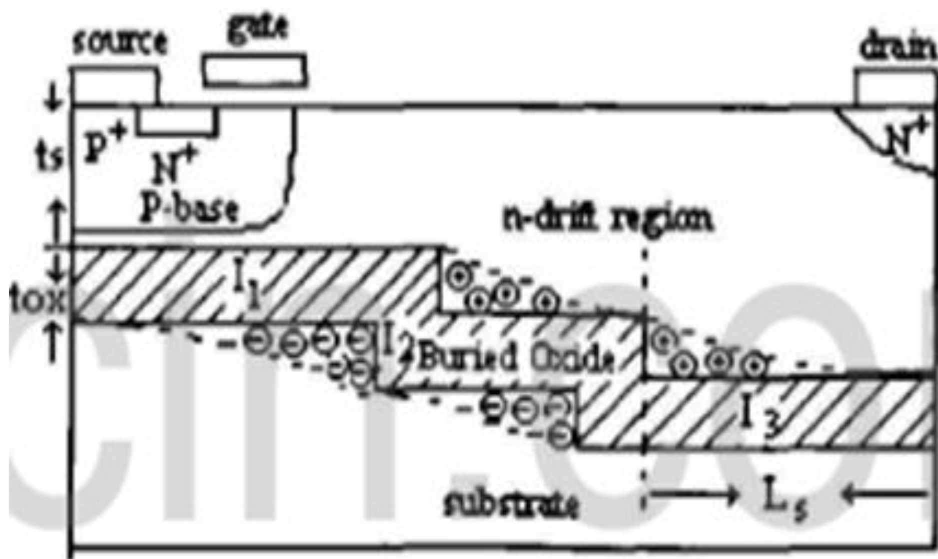

Fig.15 Buried oxide double step SOI[40]

2-2-3-4 Buried diode structure SOI

In the P-type Silicon substrate directly beneath the drain, make an N^+-doping, then the N^+P forms a reverse biased diode under reverse operation of the original device to generate a vertical electric field. is the structure is shown in Fig.16. [42]

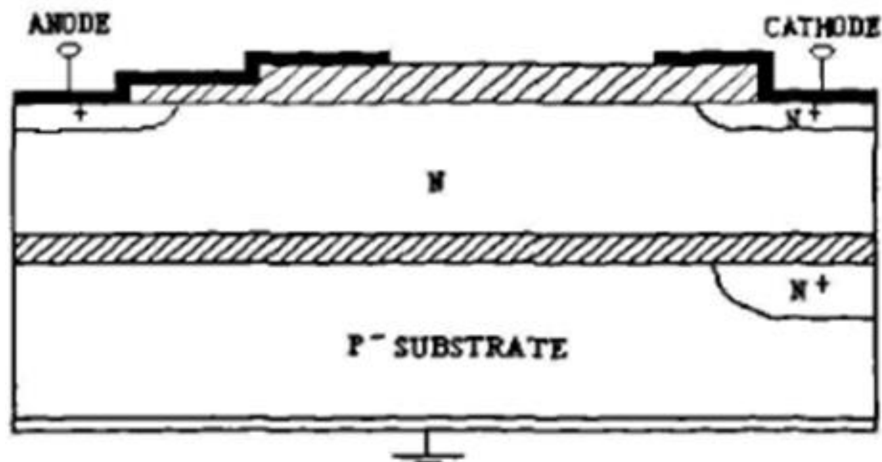

Fig.16 Buried diode structure SOI[42]

2-2-3-5 Partial SOI

The substrate is connected to the drift region right beneath drain, then the vertical electric field is increased and the breakdown voltage is enhanced. The structure is shown in Fig.17. [43]

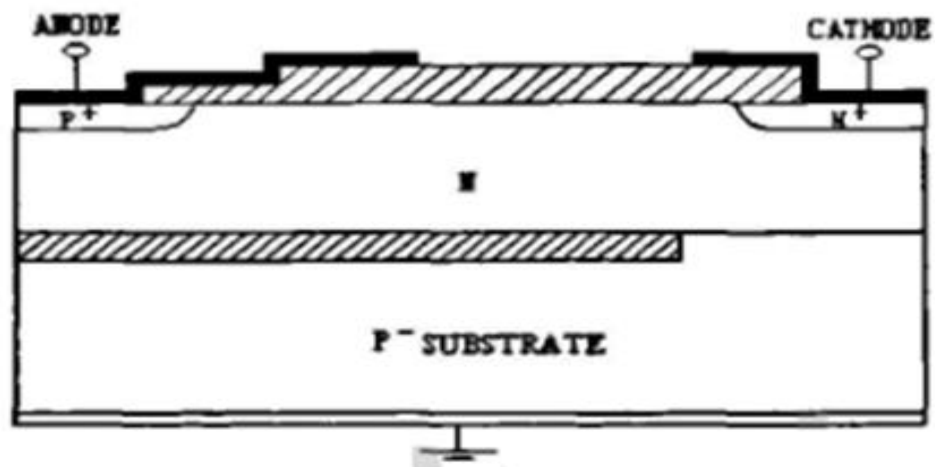

Fig.17 Partial SOI[43]

Above structure is similar with the BAGS, the gap is low-k material that equivalent to a combination of BAGS SOI and Partial SOI.

CHAPTER 3 Principle and simulation of power SOI device

3.1 Reverse biased breakdown.

The utmost efficiency of power device is the minimum of turn-on resistance and the maximum of breakdown voltage, but they are contradicted with each other. If we want to know the optimization of breakdown voltage, we need to know the principle of the reverse biased breakdown. The following are introduction of several situation of breakdown.

3-1-1 Avalanche breakdown

Avalanche breakdown occurs in reverse biased pn-junctions. The device has little current flow under reverse bias, it almost be an open circuit. While the applied reverse voltage increases, electrons that are pulled from their covalent bonds are accelerated to great velocities in the deletion region. These electrons knock off more electrons to cause more impact ionization of electron-hole pairs. They, too, are accelerated and the process repeats itself, and thus additional current. That's like an avalanche where a small disturbance causes a whole

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mountainside of snow to come crashing down, so, this is why we call this situation Avalanche breakdown. The illustration of avalanche breakdown is shown in Fig.18. [44], [45]

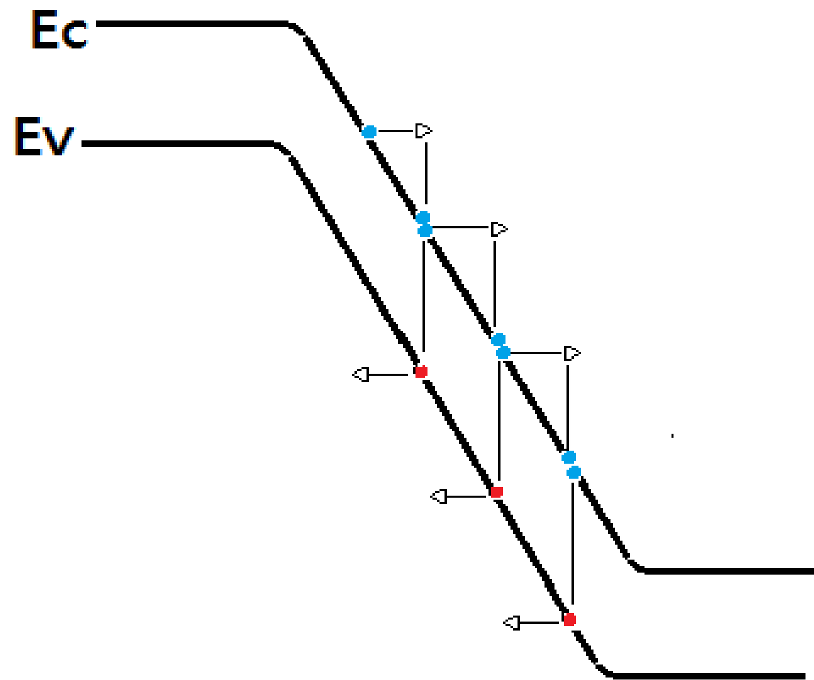

Fig.18 Avalanche breakdown

3-1-2 Zener breakdown

Zener breakdown occurs in heavily doped pn-junctions. The valance band and conduction band are much closed under reverse bias in the heavy doping situation that makes the depletion layer extremely thin. With the depletion layer thin enough, the tunneling effect occurs. The tunneling effect causing the electrons move through the junction barrier freedom, hence, the breakdown occurs. In general, the Zener breakdown works in the low applied voltage. The

illustration of Zener breakdown is shown in Fig.19. [44], [46]

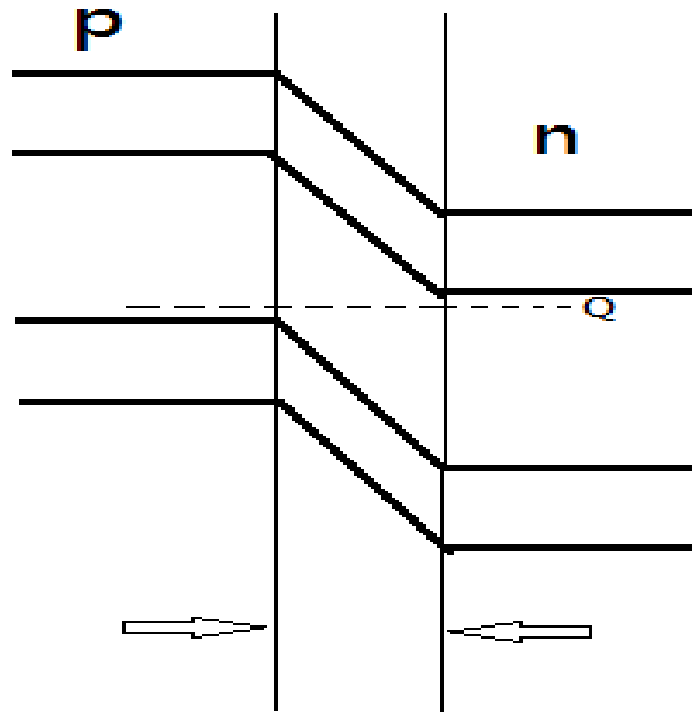

Fig.19 Zener breakdown

3-1-3 Punch-through breakdown

The punch through breakdown is easily caused in devices has the structure of NPN and/or PNP, especially when the middle material is thin. The deletion region under reverse bias will be extended to the other PN junction, when the depletion regions connected, the barrier became lower, and then the current can easily flow through this junction. With a short channel NMOSFET as an example, when the drain voltage is too large, depletion region will reach the source, current suddenly increases. Punch-through is differentiated from

junction breakdown in that the current path is from drain to source instead of from drain to substrate, as is the case for junction breakdown. [47], [48]

3.2 On-resistance

The definition of on-resistance of power devices is the resistance from cathode to anode in the turn on situation. Because the on-resistance decided how much turn on power is consumed, it is an important parameter for power devices. The power consumption of power device can be expressed as:[49]

$$P_d = I_d \times V_d = {I_d}^2 \times R_{ON} \quad (3\text{-}1)$$

The power consumption divided by the device area can be expressed as:

$$P_d/A = {J_d}^2 \times R_{ON,SP} \quad (3\text{-}2)$$

The J_d is the density of turn on current, $R_{ON,Sp}$ is specific on resistance. They are made by anode diffusion region resistance, cathode diffusion region resistance, and drift region resistance:

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$$\text{Ron,} = R_{Anode} + R_{cathode} + R_d \quad (3\text{-}3)$$

The specific turn-on resistance is defined as: $\text{Ron, sp} = \frac{V}{I/um} \times \frac{\text{UNIT CELL AREA}}{\text{CHANNEL WIDTH}}$

$$\text{Ron} = \frac{\text{Ron,sp}}{\text{DIE SIZE}} \quad (3\text{-}4)$$

3.3 The operating area of SOI

We use the simplest structure, a diode, to design our proposed device. First of all, we investigate the conventional SOI diode under the turn off situation which means device can not generate the turn on current.

We have to inspect the situation when we apply bias voltage on cathode, to fully understanding the SOI diode breakdown mechanism. The effect under low bias voltage applied to cathode was analyzed in Fig.20 (a).

When the voltage on cathode is low, the depletion region is the same as conventional device which locates between the junction of p^+-region and the n-drift region, some minor region above the buried oxide in the drift region I also depleted. When the bias voltage is increased, the depletion region extended into the n-drift region from both the p^+-direction and the buried layer direction The maximum electric field still locates at the p^+ and drift region junction, and

some neutral region still surrounds the N^+ region, see Fig. 20 (b). When the bias voltage on cathode side keeps rising until reaching the secondary pinch-off voltage, the drift region is fully depleted. The breakdown right now is determined by the n^+-n junction and the buried layer-n junction. [50] After fully deplete, we keep increasing the voltage on cathode, then we discover that the electric potential lines below the cathode become more and more crowded. In the end, the high electric field will shift from beneath the anode to beneath the cathode, Fig. 21. This is the reason why the vertical breakdown occurs easily in the lateral SOI power devices. We can prevent device from breakdown early by reducing the high electric field in the horizontal direction which is located at the p^+ and n-drift region junction and increase the breakdown voltage of a high power device by reducing the vertical electrical field which is located at the n^+ and n-drift region junction in conventional SOI devices.

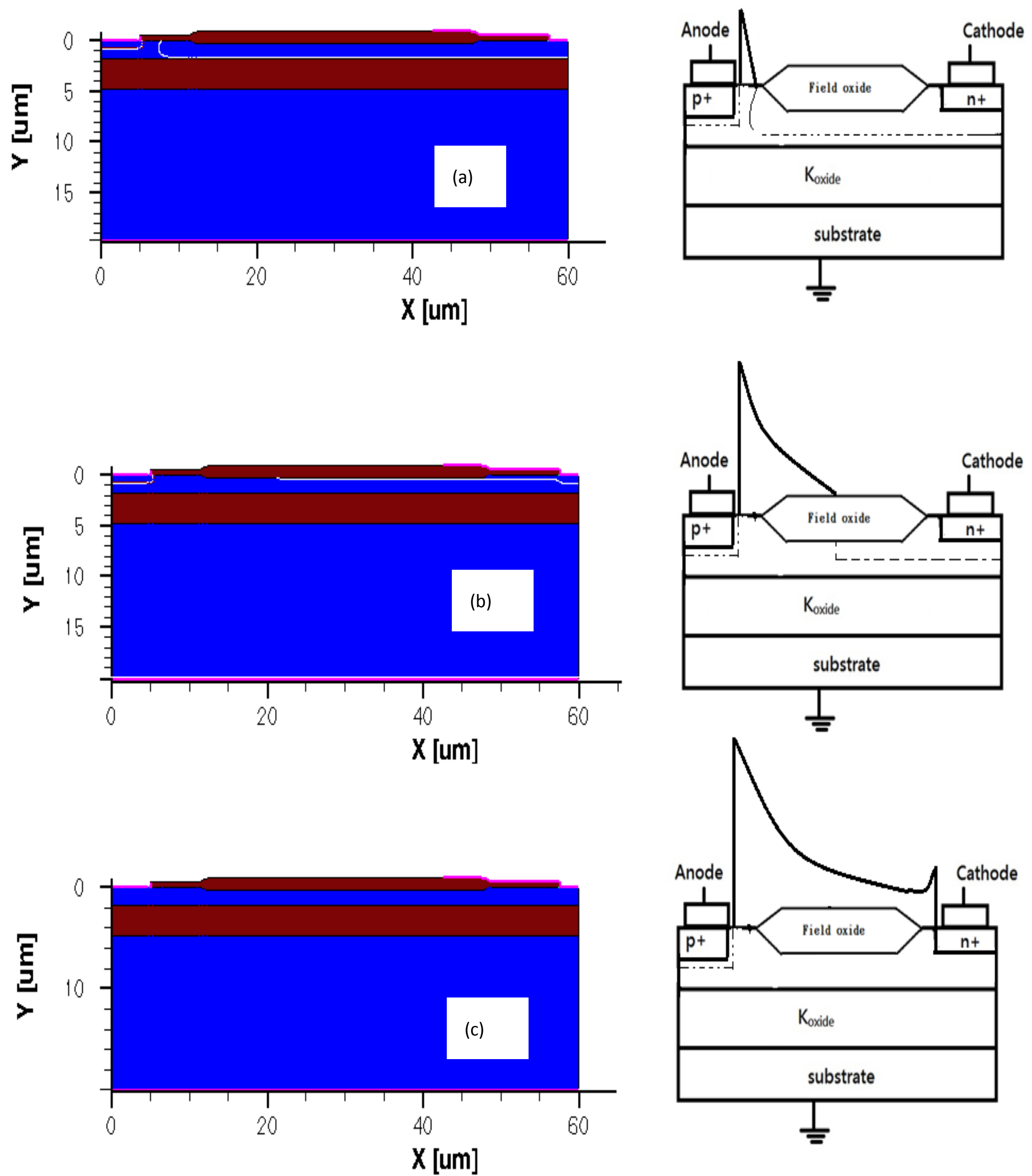

Fig.20 Reverse biased depletion region in an SOI diode for (a) low voltage, (b) medium voltage, and (c) high voltage.

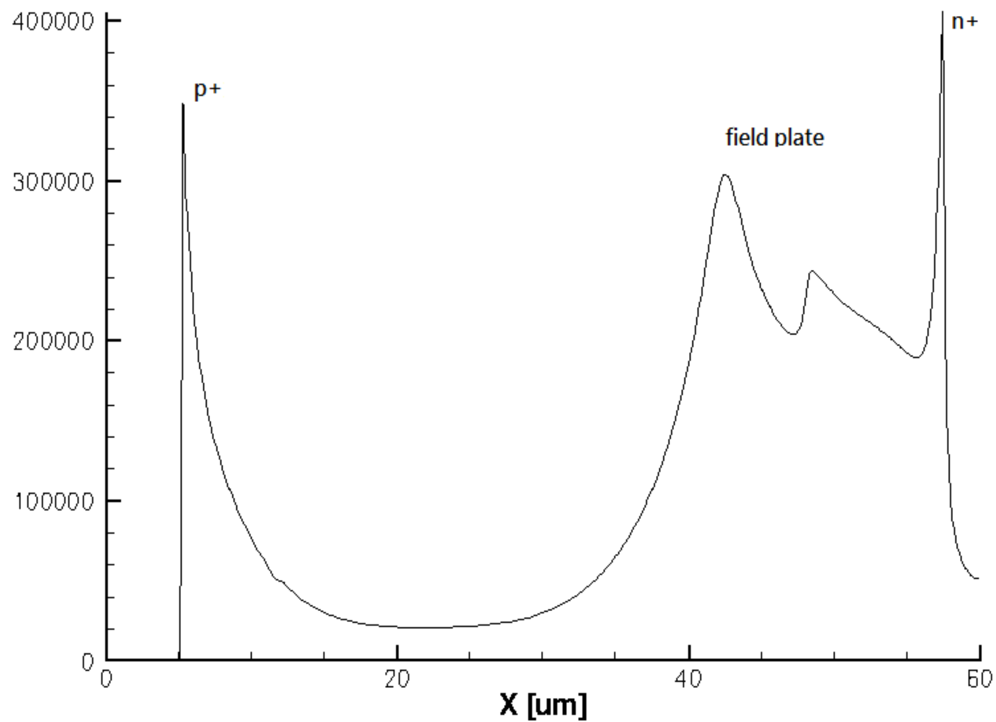

Fig.21 The surface electric field of a lateral SOI power device.

3.4The simulation of lateral power SOI devices

We know from the literature review that the oxide layer thickness and epitaxial layer thickness can impact the breakdown voltage. However, the dose concentration and drift region length, too. Our proposed device is based on the smart-cut technology, so we have a thin SOI that can combine the low voltage devices in a single chip. However, when the epitaxial layer thickness is decreased the on-resistance of the power device will be increased, so we chose the thickest silicon layer of smart cut wafer available in Fig.8. The simulation size of our proposed SOI silicon layer is 1.5 μm.

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3-4-1 Doping concentration & breakdown voltage

Fig. 22 shows the breakdown voltage under different silicon layer concentration, when the concentration is not too high, the breakdown voltage will increase follow the doping concentration. When the concentration over the specific value, the breakdown voltage will decrease with the epi-layer concentration.

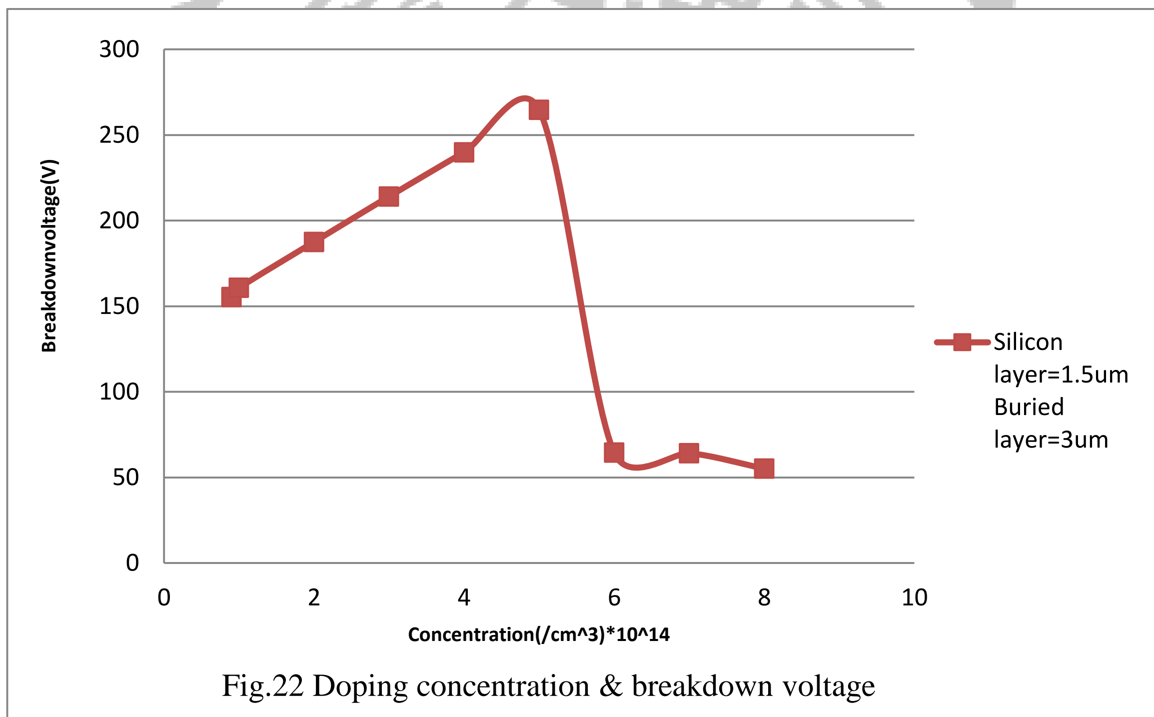
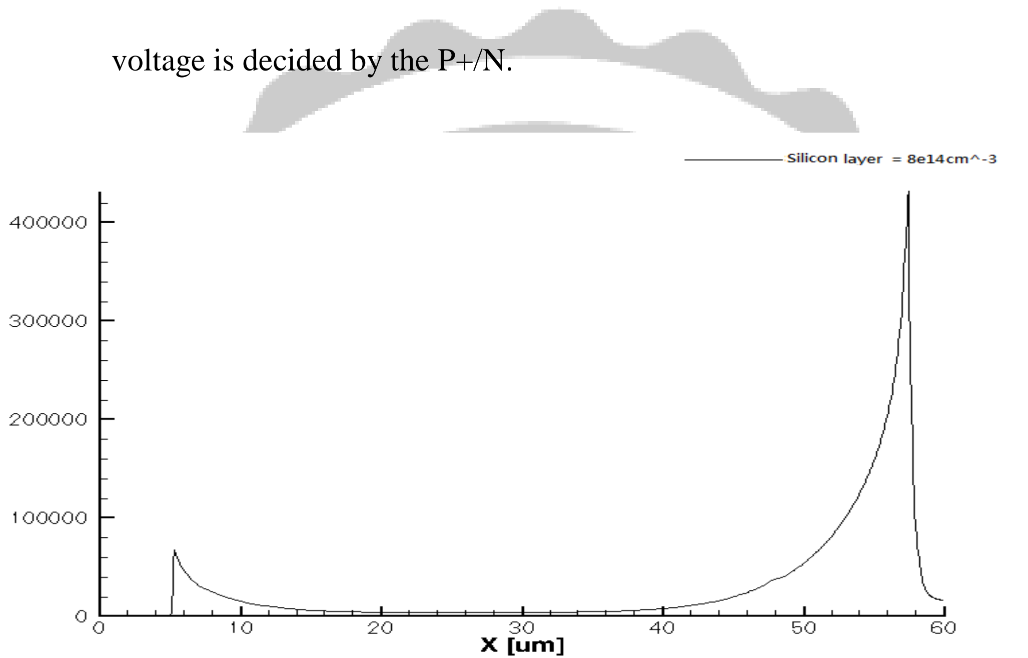


Fig.22 Doping concentration & breakdown voltage

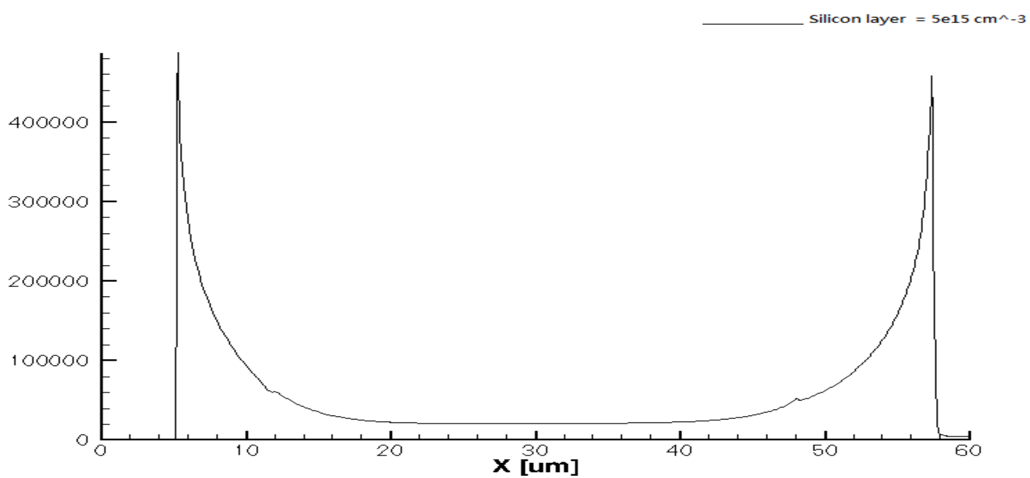
Fig. 23 shows the electric field under different concentration. The low concentration will cause full depletion early and the rate of P^+/N^- rise slowly, so the breakdown is occurred at the N/N^+ junction, see Fig. 23(a).

When the concentration of silicon is increased, the electric field is shown in Fig. 23 (b). It's an ideal situations, the electric field is more uniform. When the

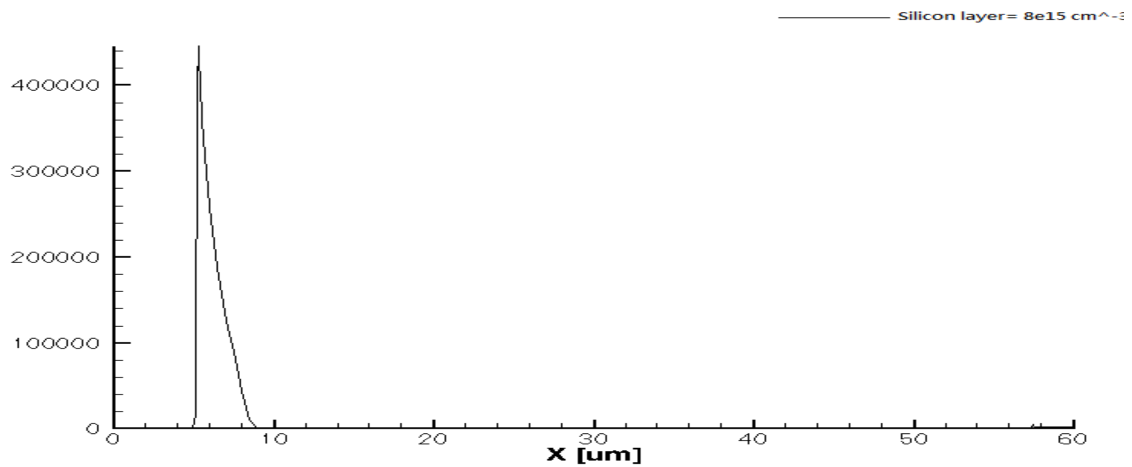
concentration is further increased, the electric field is shown in Fig. 23(c). The depletion region does not extent into the n-drift region too much, due to the high doping concentration, the electric field piles up at the junction quickly, and results in a lower breakdown voltage. horizontal junction. The breakdown voltage is decided by the P+/N.



(a)



(b)



(c)

Fig. 23 The electric field under different concentration, (a) low concentration, (b) medium concentration, and (c) high concentration.

3-4-2 Buried oxide thickness & breakdown voltage

Breakdown of device is determined by P^+ and drift region junction when it is not fully depleted. After fully depletion, it will be determined by the thickness of buried oxide. The buried oxide is thicker, the voltage that across the oxide will be higher, the breakdown voltage will be rise, as shown in Fig.24. Fig. 25(a) is the electric field of buried oxide layer which below the cathode.

As we can see in Fig. 25(b), the thinner the buried oxide is, the higher electric field will be. On the other hand, the higher the electric field of buried oxide layer is, the higher the electric field of silicon epi will be. When the oxide is thicker, the electric field below the cathode can be disperse which make it won't breakdown early.

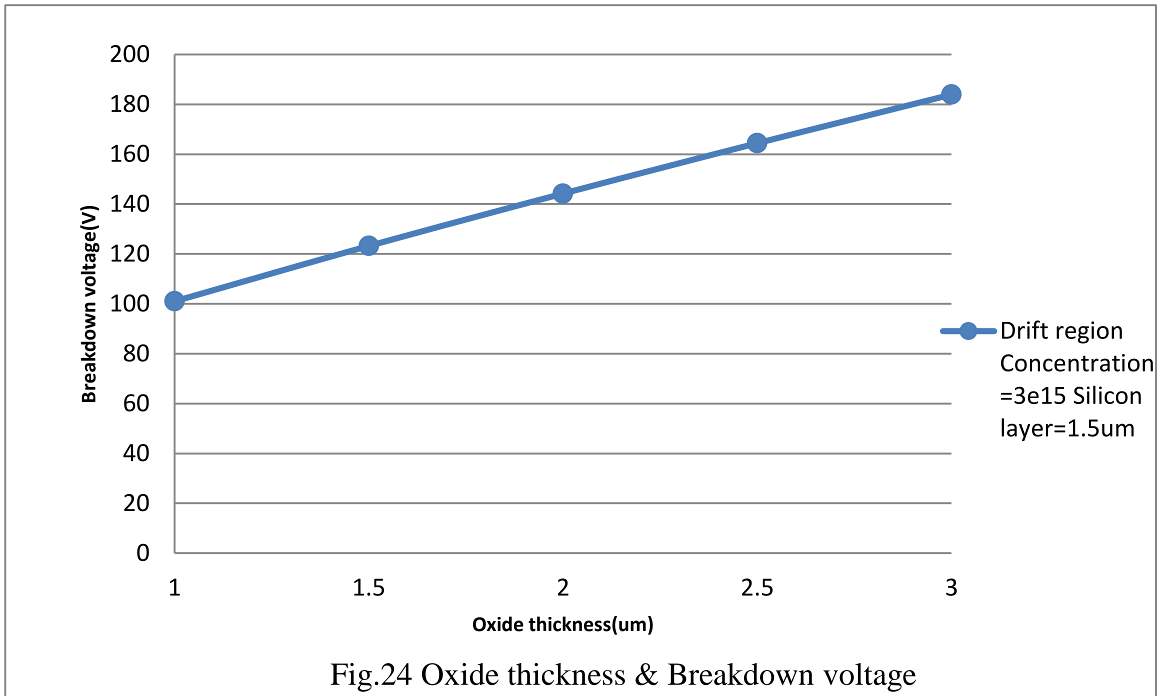
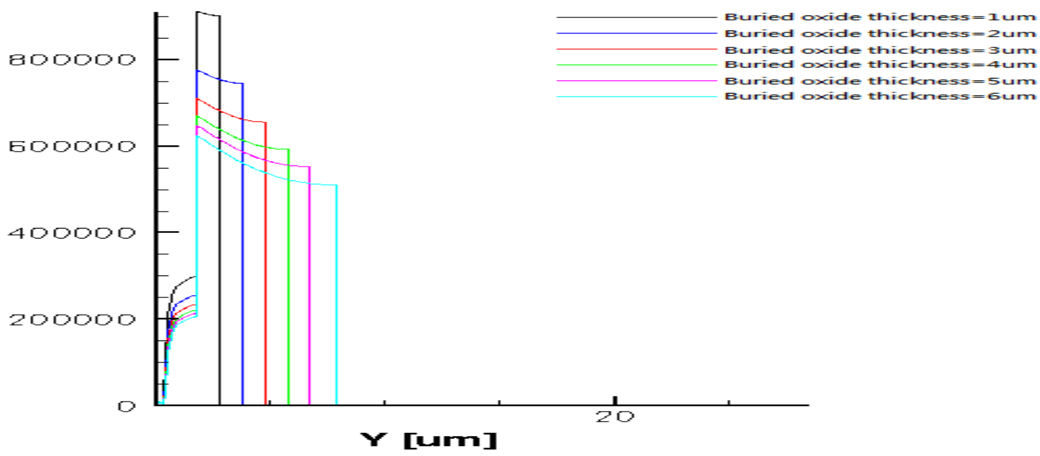
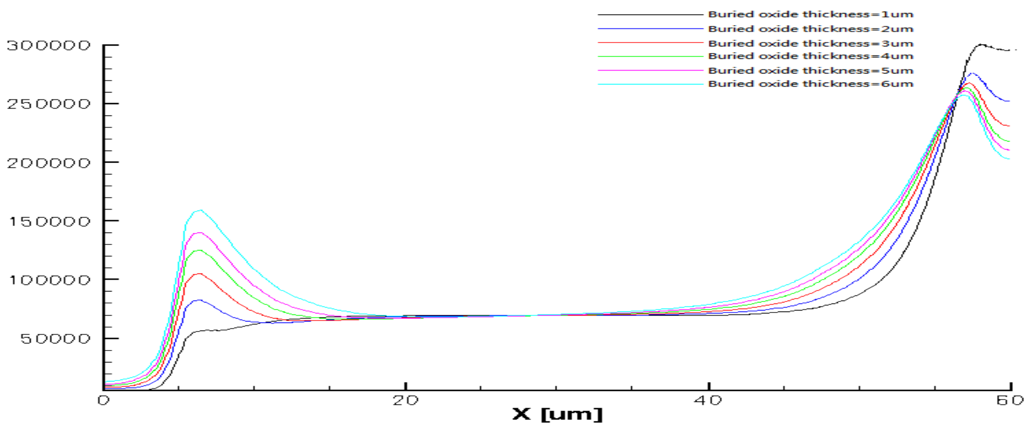


Fig.24 Oxide thickness & Breakdown voltage



(a)



(b)

Fig.25 Oxide thickness & Electric field

3-4-3 The optimized doping concentration & buried oxide thickness

To obtain maximum breakdown voltage, increase the thickness of oxide will be advantageous, but it's not good for on-resistance. Because when we increase the thickness of oxide, the doping concentration for maximum breakdown voltage should be decreased, that will make the on-resistance increase. The result is shown in Fig.26.

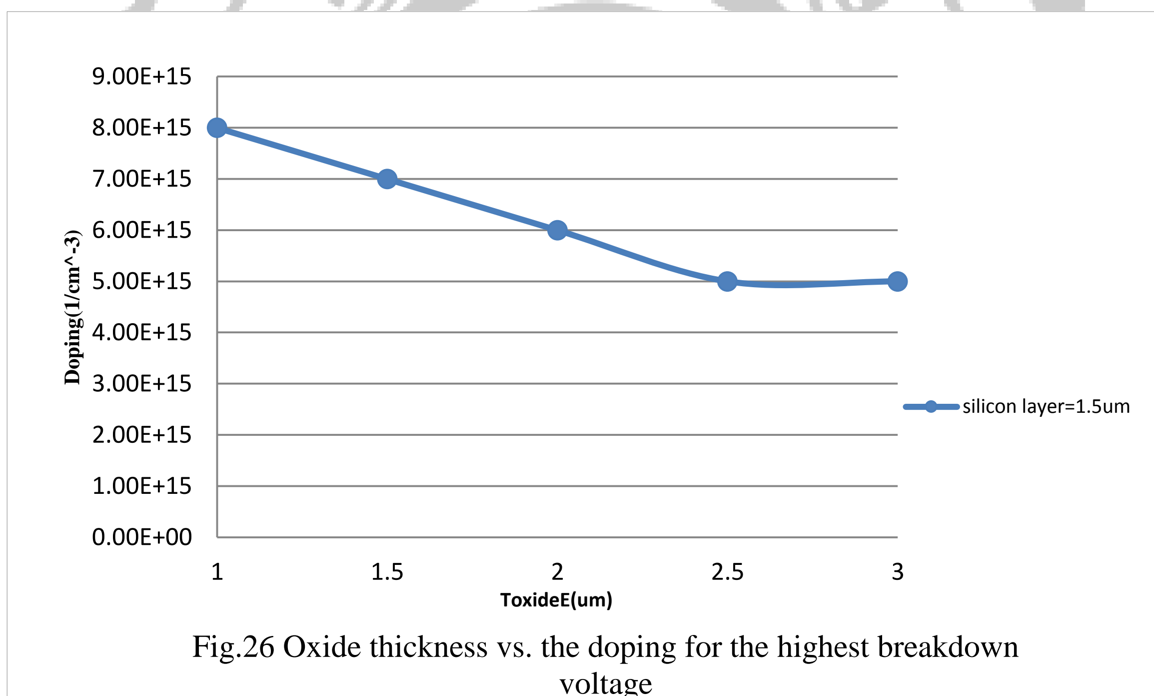


Fig.26 Oxide thickness vs. the doping for the highest breakdown voltage

CHAPTER 4 Better performance with low-k dielectric material

4.1 Concept of proposed SOI power device

From the mentioned structures in Chapter 3, it can be seen that the most effective ways to improve the intensive electric filed is to adjust the electric field below Drain. To prevent the resistance increase in the epitaxial layer, almost all of the researchers choose to use the buried oxide layer or the substrate to influence the electric field indirectly.

The buried oxide layer of SOI limits the vertical electric field, enhancing the vertical electric field is also an important research direction.

Due to the above collected SOI model and the feasibility of Smart-Cut technology, this thesis will present some concepts in this chapter to develop a high voltage thin SOI device that can compatible to the CMOS technology.

The concept of this structure is to increase the electric field in the buried dielectric by using a low k composite dielectric. To Enhanced the vertical electric field of buried oxide layer to reduce the lateral electric field of epitaxial layer.

The above-mentioned method is used in the buried air gap structure (BAGS)

that has a segment of air area in the buried dielectric. The range of the breakdown voltage is limited, so we propose a new structure that has alternated SiO_2 and air with different widths and spacing.

4.2 Device structure

The proposed device structure is based on the conventional SOI which has the best breakdown voltage under a fixed length. First of all, we will find the optimal concentration of the drift region, and the position of field plate, locos and so on. The design of proposed structure is based on Fig.6. As we can see in the figure, the maximum length and thickness in the smart-cut technique is to fix the R-on. First of all, we simulate the conventional SOI which the sizes are 1.5um epitaxial thickness and 3um buried oxide thickness.

LA and LB in the conventional SOI which shown in Fig.27, are the same size in those three devices. LA is the length of field plate which can determine the place of electric charge accumulation. The electric charge accumulation can generate higher surface electric field. Therefore, LA is an important parameter. After fixing LA, we focus on LB. LB is the length between cathode and locos which generate the electric charge accumulation, too. This length couldn't be too far from cathode or it couldn't affect. However, it couldn't be too short or

it may cause early breakdown. Table 1 is the concentration of the drift region, device size, and the optimal LA and LB in the conventional 120 um SOI.

Table 1. Device parameters used in TCAD simulation

Parameter	Value
Device Length (μm)	120
T_{epi} (μm)	1.5
T_{ox} (μm)	3
Drift region concentration (cm^{-3})	4e15
LA(μm)	35
LB(μm)	20

The difference between conventional SOI and BAGS SOI is that the buried layer of BAGS is made of two dielectrics, one of which is SiO_2 and the other is air. It is shown in Figs. 28 and 29. Therefore, an electric field peak will occur at the intersection. By adopting suitable pattern design, the air and oxide alternating will be under control, the electric field distribution in the Si epi-layer becomes tunable by the pattern design of this SiO_2 etching mask .It is shown in Figs. 30 and 31. BAGS and the proposed structure both have the low-k dielectric buried layer (air). But they are different from that proposed structure has more graded segments of low-k areas. The main position of

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patterned design is located between cathode and field plate, and we maintain the air region between field plate and the nearby anode patterned. The place where have more electric charge accumulation will generate lopsided electric field, thus why we used patterned structure to reach uniformity. The details will be discussed in the following chapter. Before the bonding process, the buried SiO_2 layer is selectively etched in the proposed structure to make it become air and oxide in an alternating form. Therefore, the electric field distribution in the Si epi-layer becomes tunable by the pattern design of this SiO_2 etching mask. The different lengths of device have the different structure, so we need to propose the structures for shorter and longer device. However, we did not analyze the length of locos and field plate in the short device. We can discover that the structure design was always located nearby the cathode because on cathode side has highest electric field in short device. In longer device, due to the electric field in the middle of drift region will fall down. We will put the designed structure nearby the anode, as shown in Figs. 28, and 30 respectively. In the following chapter, we will discuss the process and the result of simulated electrical properties.

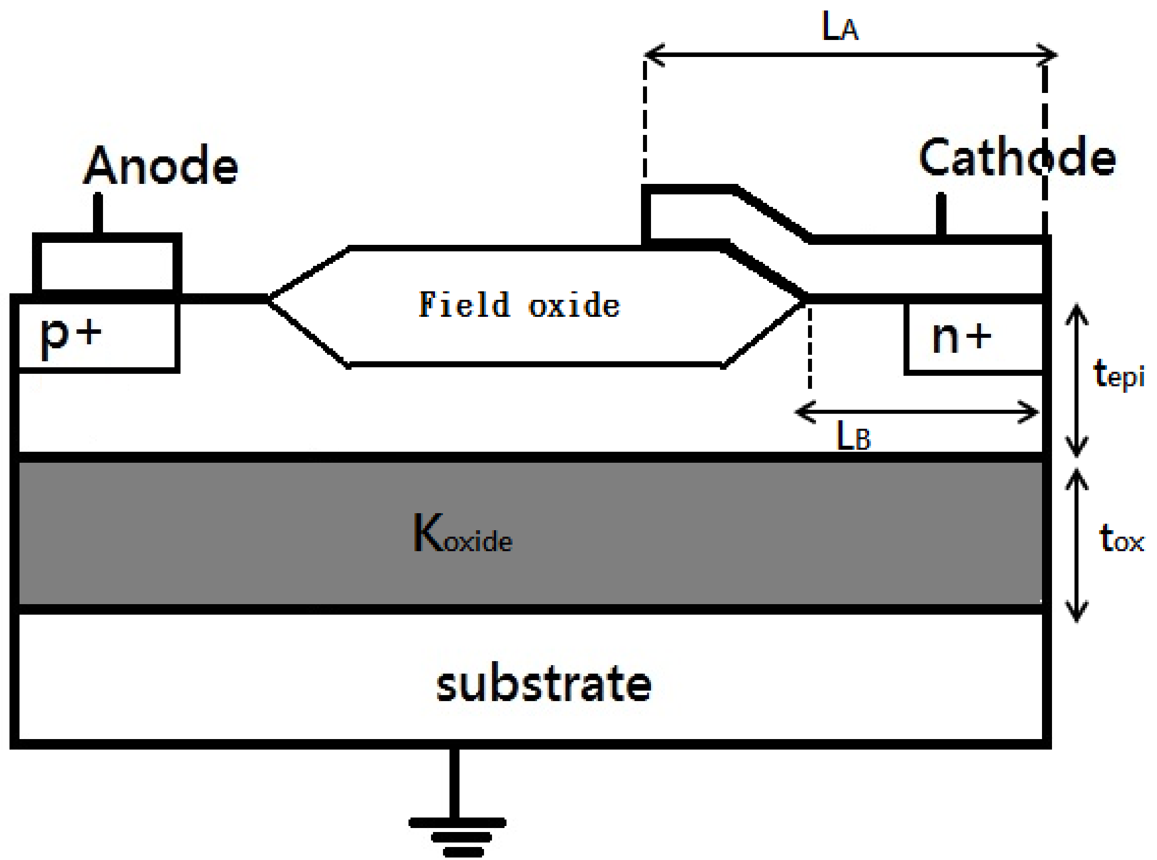


Fig.27 The conventional SOI

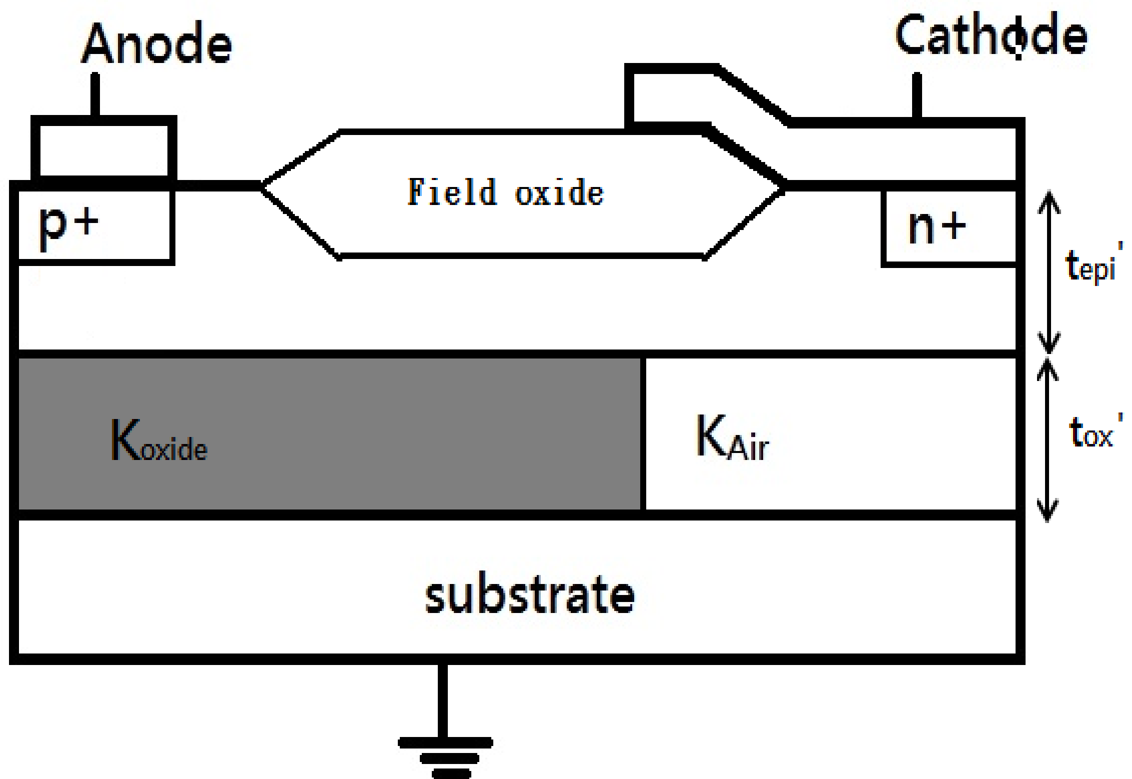


Fig.28 The shorter BAGS SOI

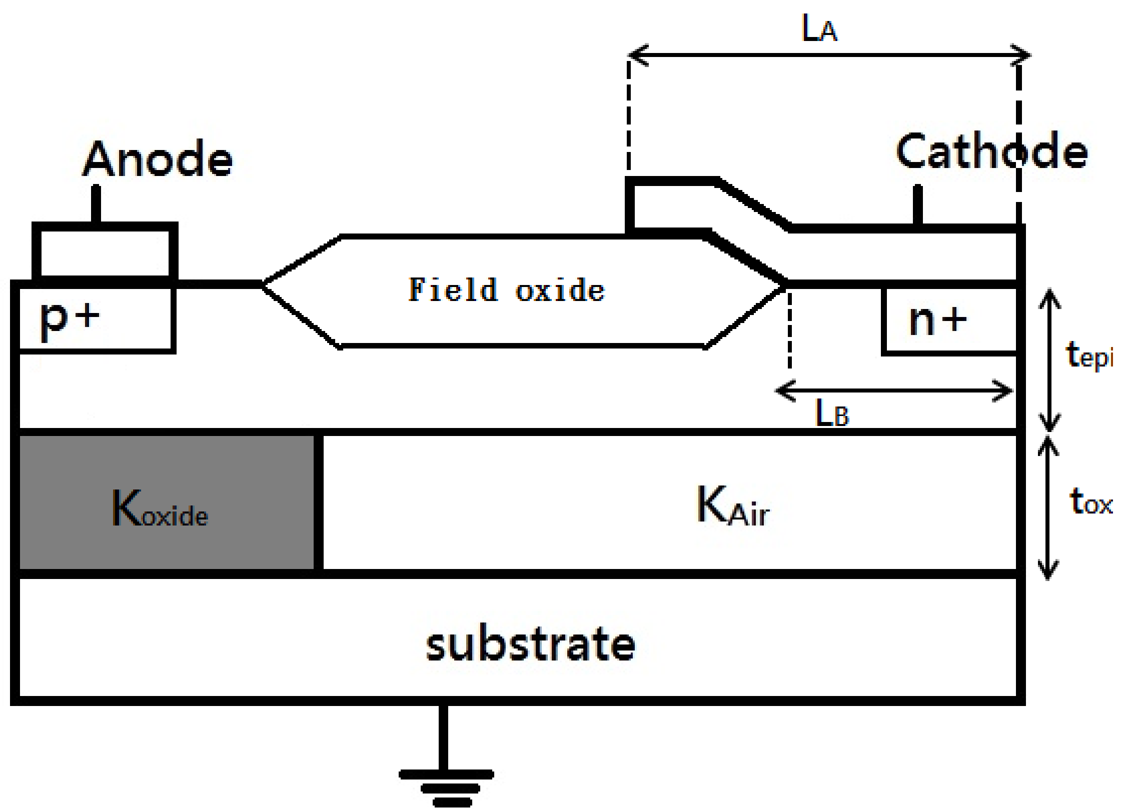


Fig.29 The longer BAGS SOI

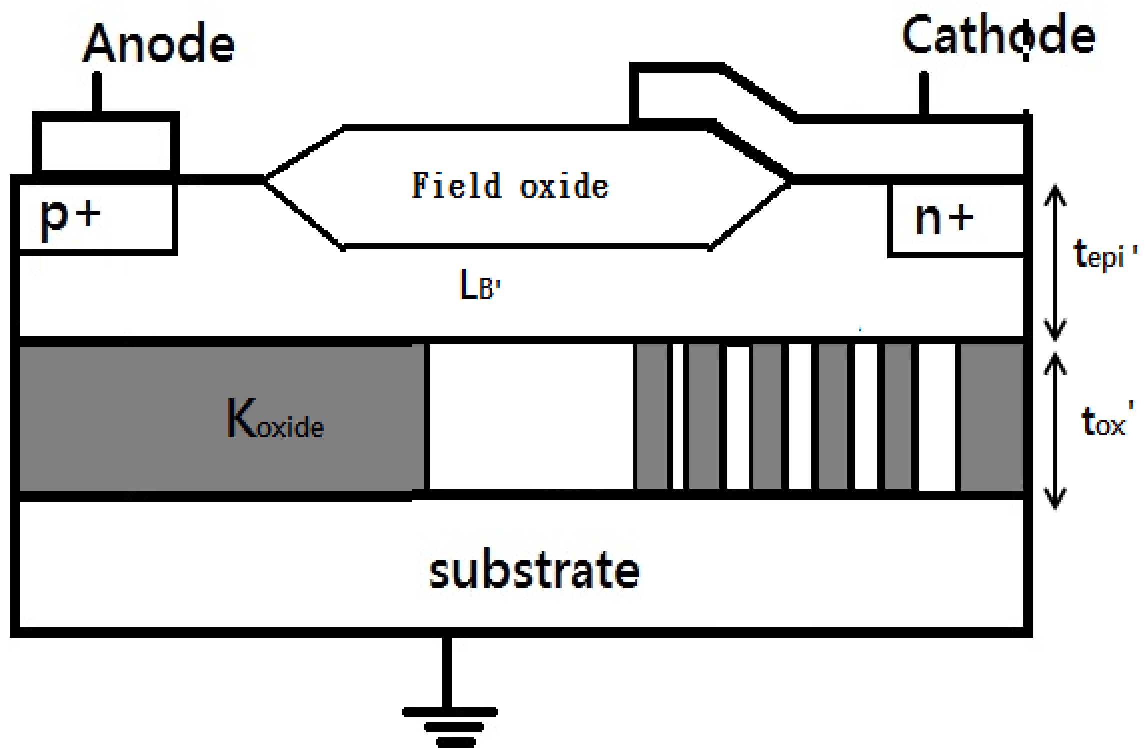


Fig.30 The shorter proposed SOI

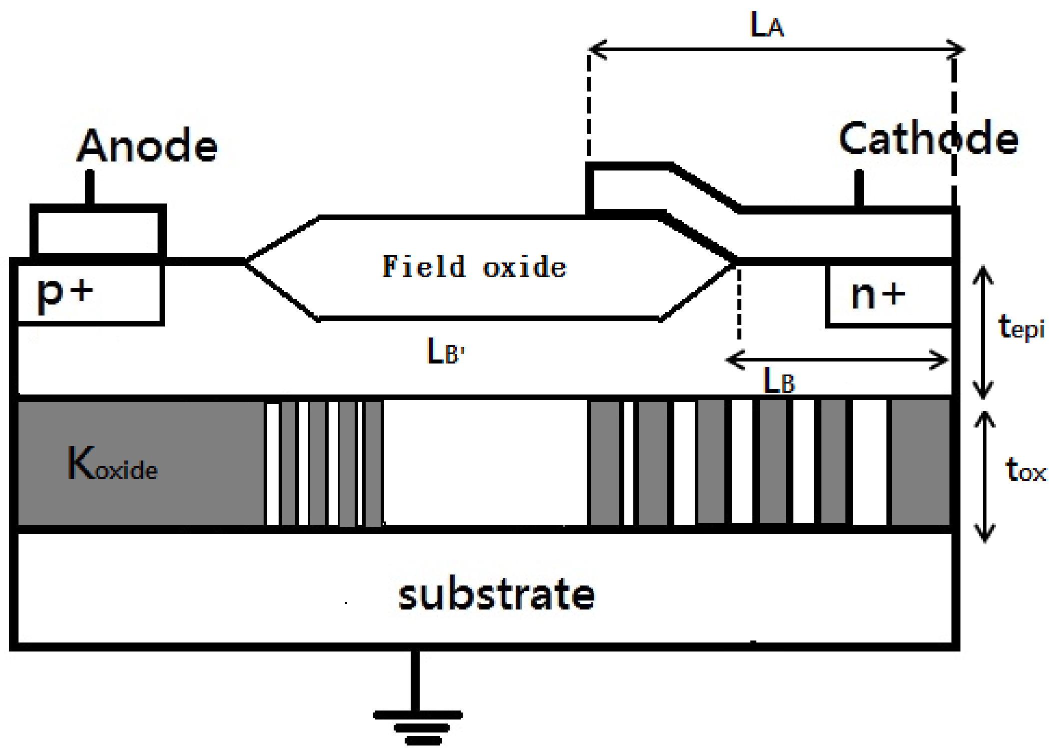
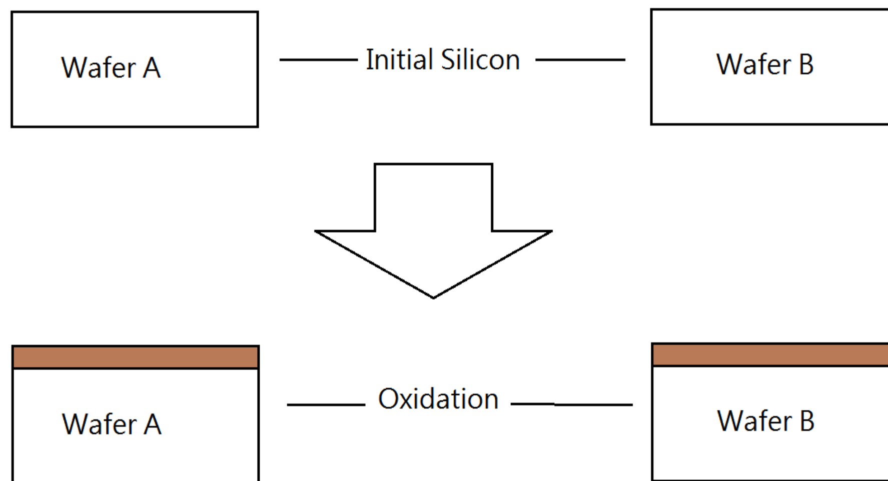


Fig.31 The longer proposed SOI

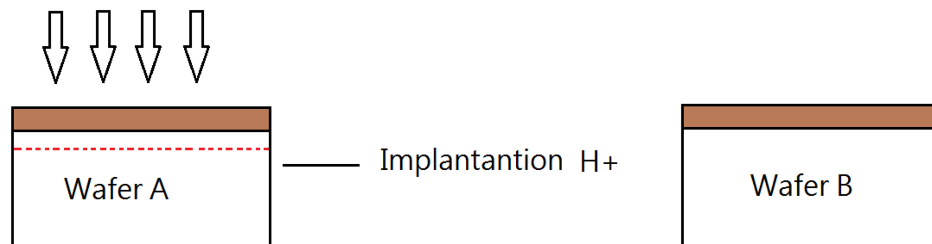
4.3 Process of proposed SOI power device

Ensure the feasibility of device is important, so we propose the process of our structure in the following steps.

Step1: The wafer A and Wafer B are grown with a thin dielectric layer of thermal SiO_2 which will serve as the buried oxide of the SOI structure.

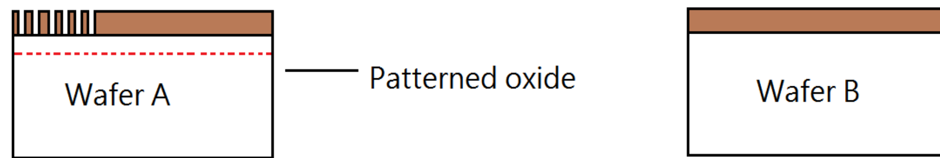


Step2: Hydrogen implantation into wafer A capped with thin layer of thermal grown SiO_2.

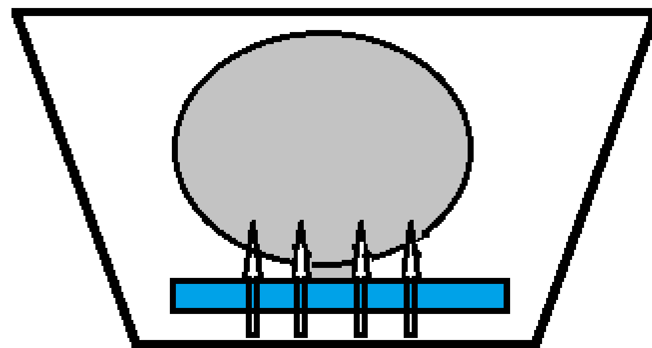


Step3: The buried SiO_2 layer is selectively etched A to make it air and oxide

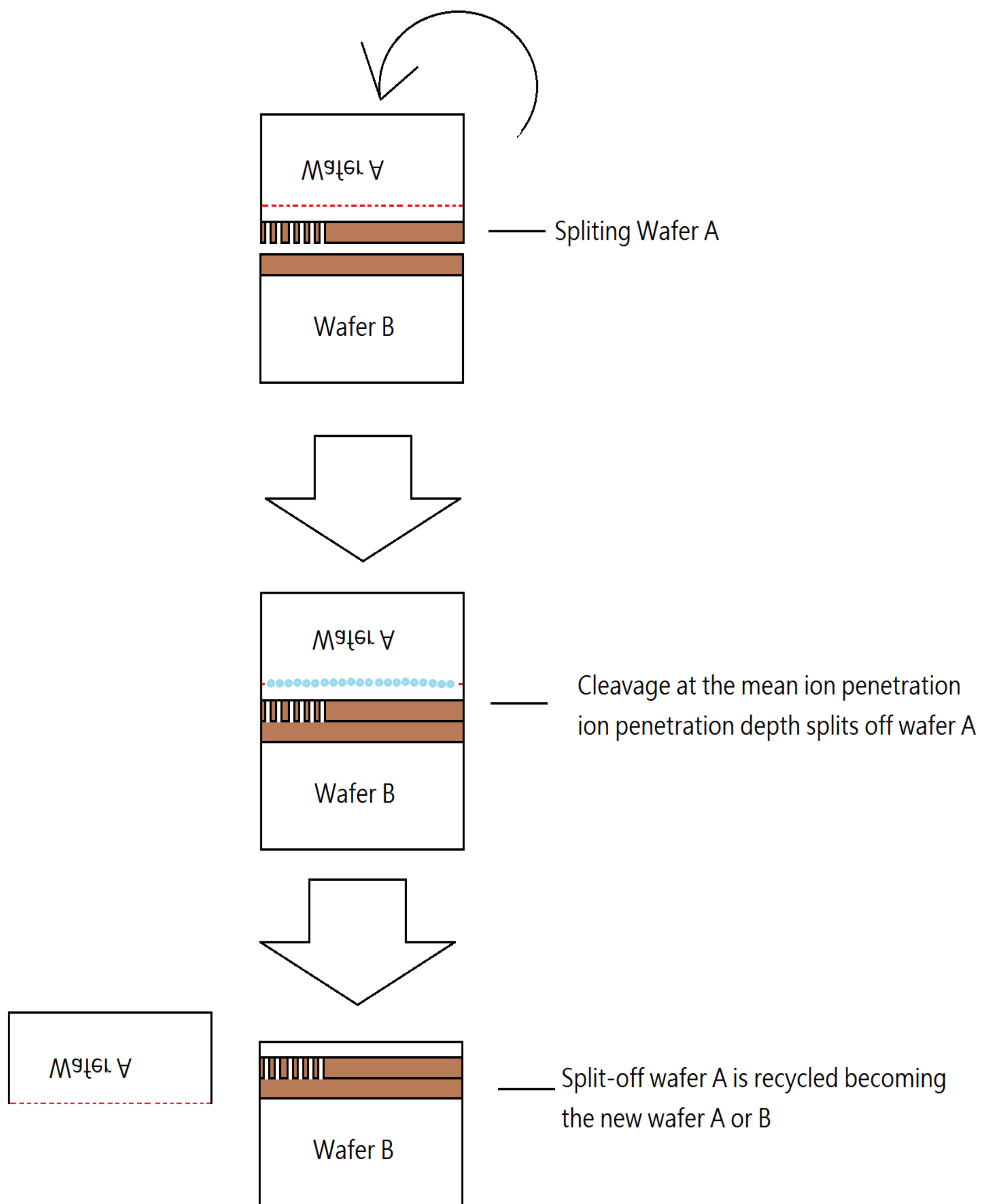
are patterned in an alternating form.



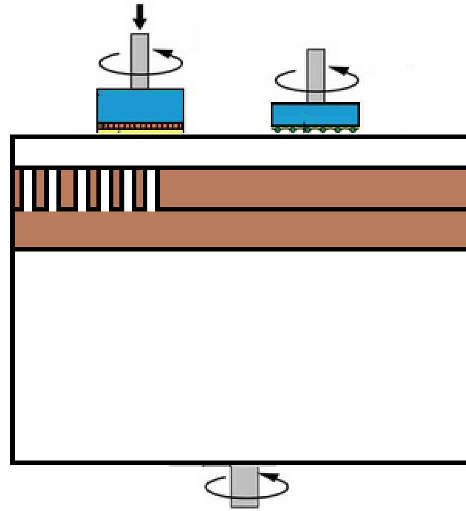
Step4: Wafer A and wafer B are cleaned using a modified RCA clean. The condition of RCA-process plays a key role in the bonding process which determines the characteristics of the surface in terms of micro-roughness hydrophilicity and particle contamination etc.



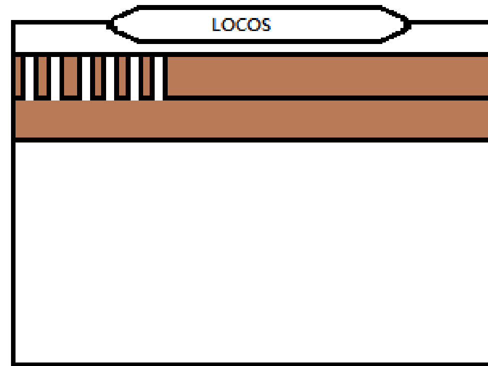
Step5: Two phase heat treatment of the two bonded wafers. During the first low temperature treatment, the implanted wafer A splits into two parts: the thin patterned layer bonded to wafer B presenting as a SOI structure and the rest of wafer A which can be recycled and used as a handle wafer again. The high temperature treatment phase is to strengthen the chemical bonds.



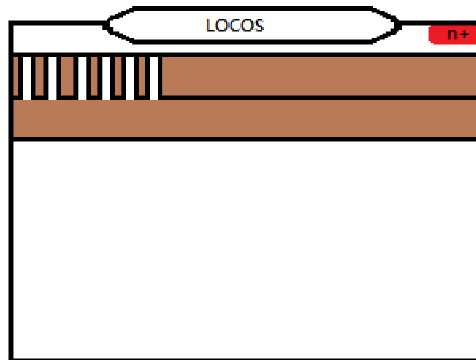
Step6: The new structure is touch polished using chemical mechanical polishing (CMP) since after splitting the upper layer of the SOI structure has a surface micro-roughness that has to be reduced.



Step7: LOCOS



Step8 Implant n^+



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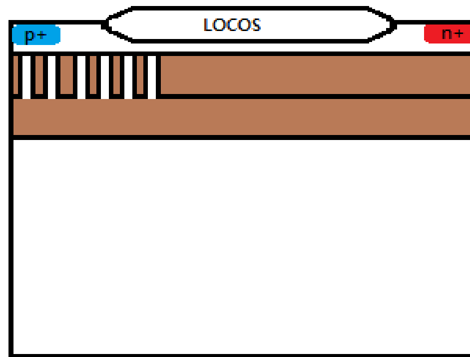
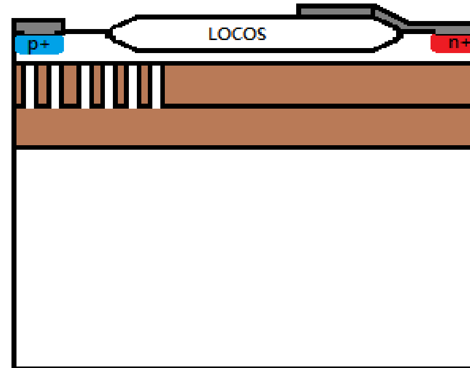
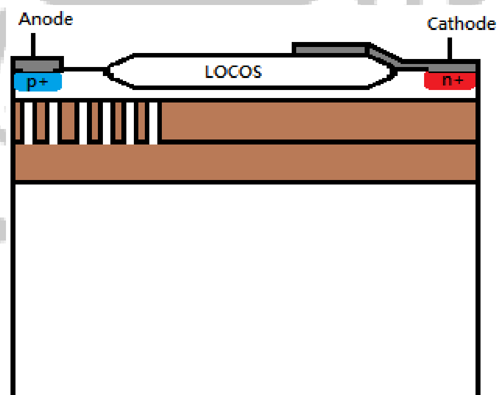
Step 9: Implant p^+



Step10: Set up metal for field plate and cathode.



Step11: Set up the electrode.



4.4 Simulated electric field distribution

Due to the operation area is discontinuous under the SOI turn off condition, we will analyze the operation area of conventional SOI, BAGS SOI, and our proposed SOI under two conditions. One is fully depletion, and the other is incomplete depletion.

Incomplete depletion:

As we know in Chapter 3-3, the highest electric field peak occurred at the P^+N intersection in the SOI which under the condition of incomplete deplete and the electric field will drift following the depletion layer. However, the highest peak didn't affect the electric field in the cathode, field plate, and locos. As shown in Fig. 32, we discover that the conventional SOI is fully depleted until reaching 120V and the electric field is more uniform at the cathode side. As shown in Fig. 33, after adding air into the buried layer. There generates a great electric field at the intersection between air and oxide. This great electric field will twist the drift region field around the intersection, as shown in Fig.33 (100V). We can see the following is directly proportional to the dielectric constant of buried oxide layer in the following pinch-off voltage formula [50] (4-1). Fig.34 is the proposed structure which adding the air into buried oxide layer. The proposed one is fully depleted earlier than BAGS due to the ratio of oxide to air is higher

than BAGS. The depletion layer which located at patterned region was affect by electric field and become jagged.

$$V_P=\frac{qNd}{2\varepsilon_0\varepsilon_{si}}\left(t_{si}^{\,2}+2\frac{\varepsilon_{si}}{\varepsilon_{ox}}t_{oxb}t_{si}\right) \quad (4\text{-}1)$$

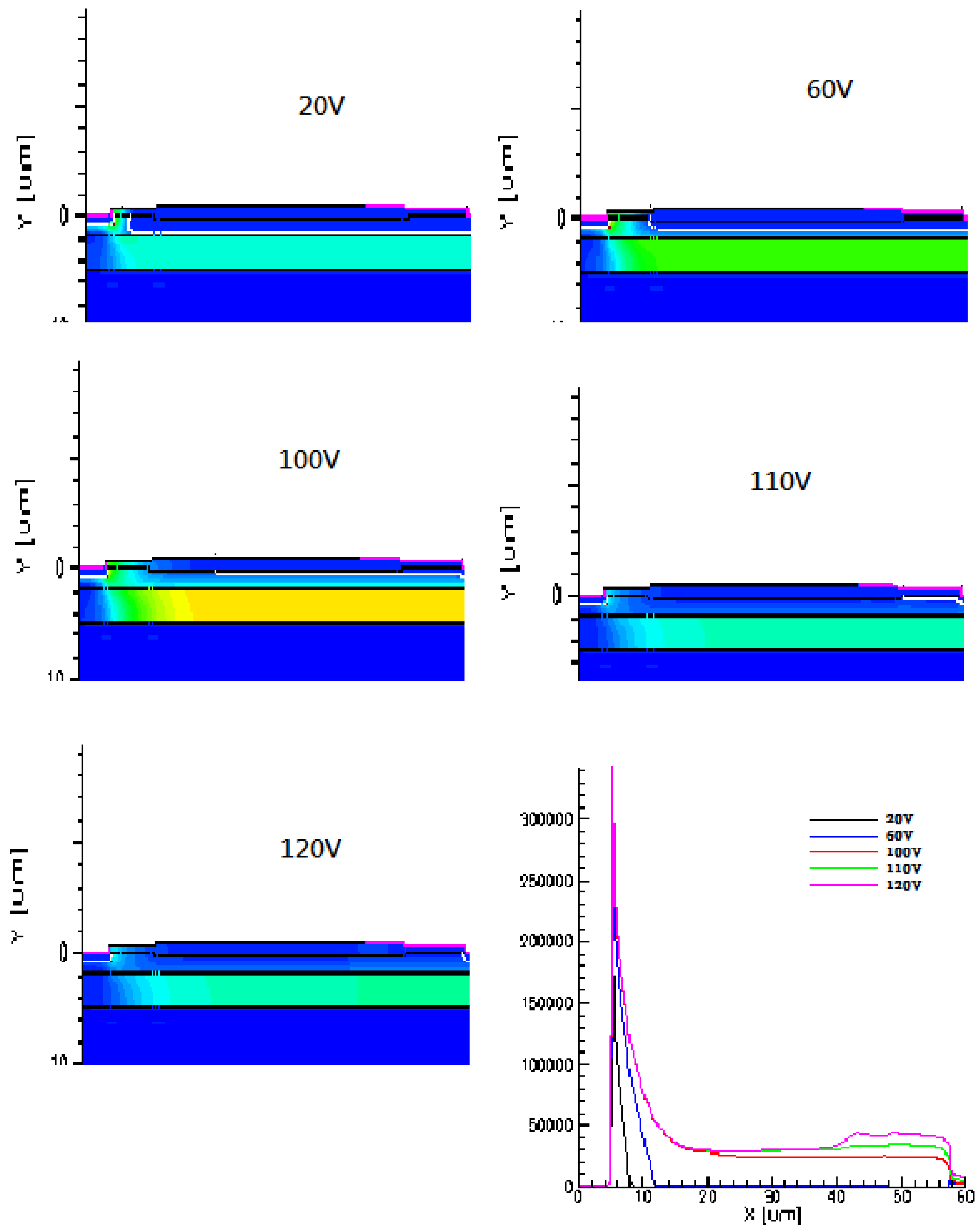


Fig.32 Depletion region with electric field of conventional SOI under different bias voltages

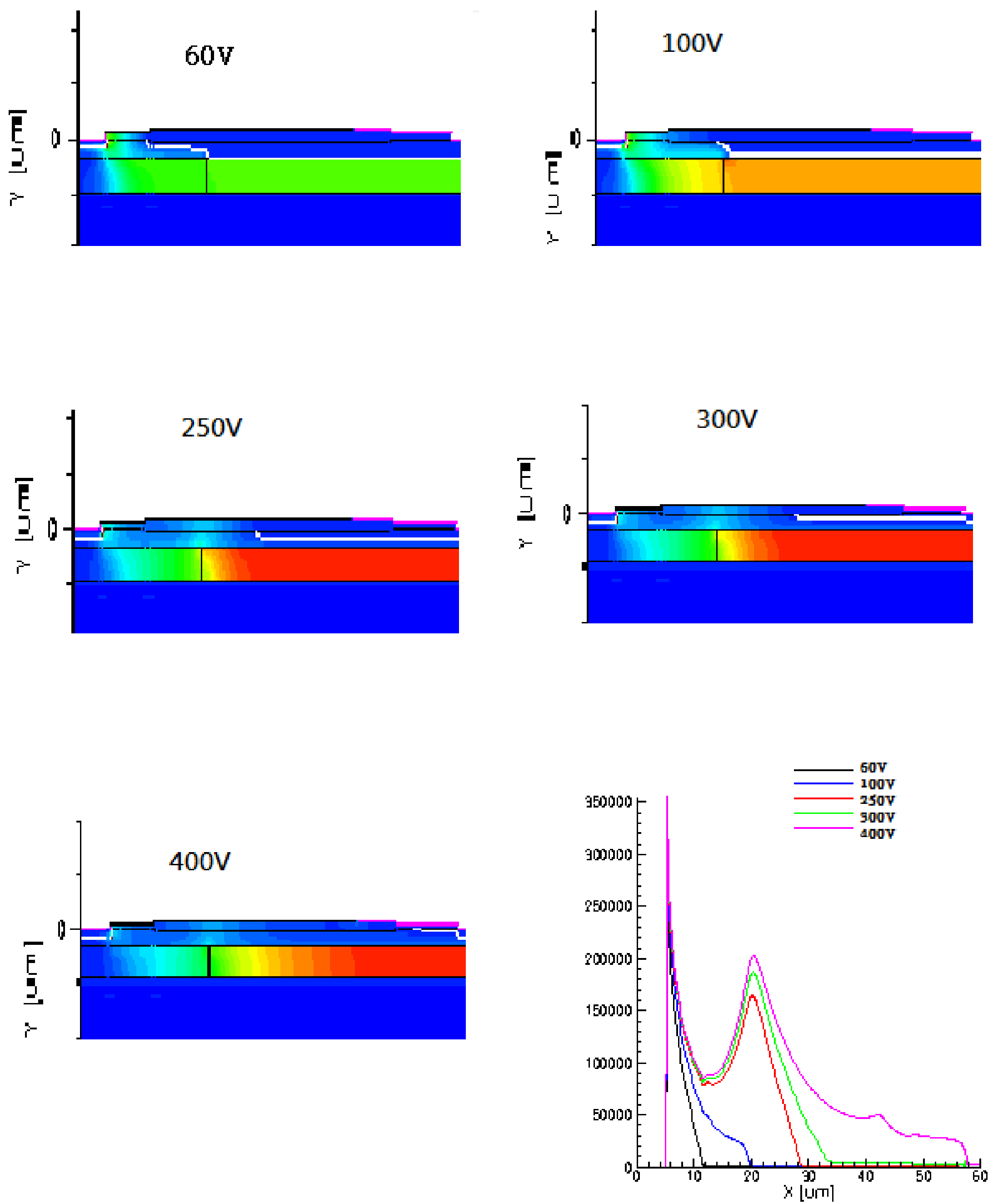


Fig. 33 Depletion region with electric field of BAGS SOI

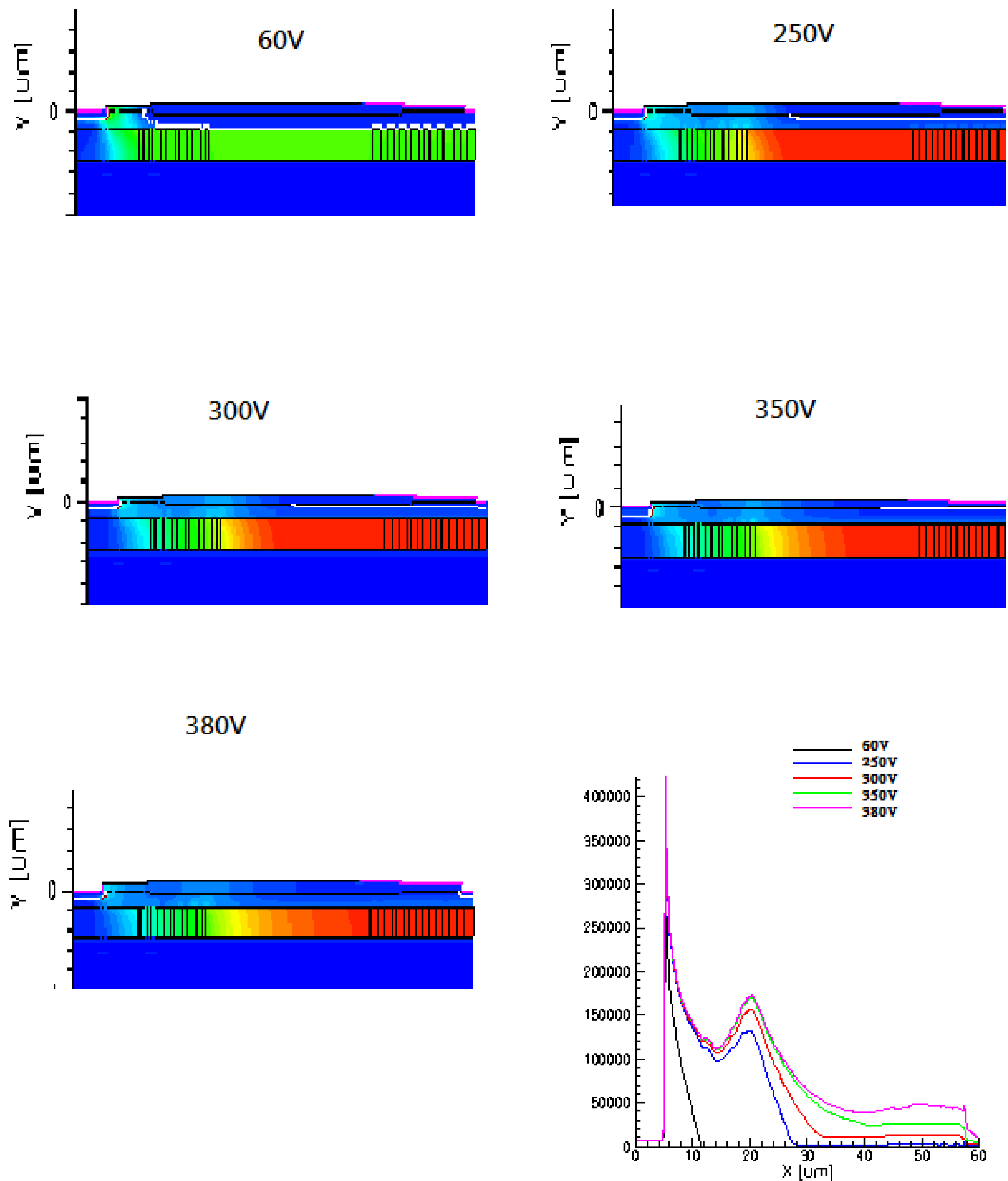


Fig.34 Depletion region with electric field of proposed SOI

Fully depletion:

In the chapter of operating area, we know that we can increase the breakdown voltage by reducing the electric field in P^+ and N^+ junction. We can analyze the electric field in conventional SOI, BAGS SOI, and the proposed SOI through different cut-lines. As shown in Fig. 35, we will analyze the electric field following the A, B, C line in the figure.

Through electric field formula:

$$E_{insulator}\ \epsilon_{insulator} = E_{silicon}\ \epsilon_{silicon} \quad (4\text{-}2)$$

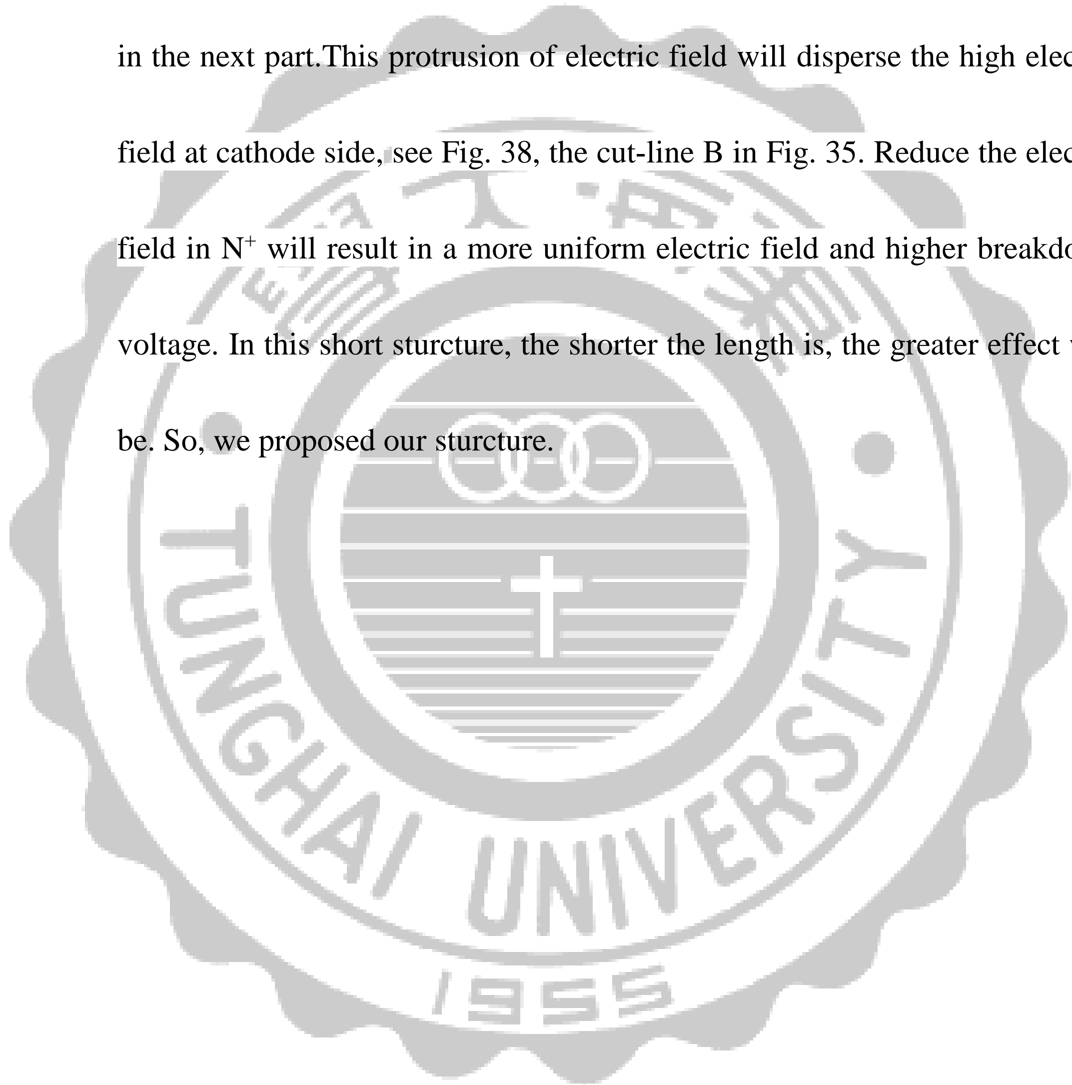
$$\epsilon_{air} < \epsilon_{oxide} \quad (4\text{-}3)$$

$$E_{silicon}: \frac{E_{air}\epsilon_{air}}{\epsilon_{silicon}} \text{ (The buried air layer) } < \frac{E_{oxide}\epsilon_{oxide}}{\epsilon_{silicon}} \text{ (The buried oxide layer)} \quad (4\text{-}4)$$

$$E_{insulator}: \frac{E_{silicon}\epsilon_{silicon}}{\epsilon_{air}} \text{ (The buried air layer) } > \frac{E_{oxide}\epsilon_{oxide}}{\epsilon_{silicon}} \text{ (The buried oxide layer)} \quad (4\text{-}5)$$

We discover that when replacing the oxide into low-k matrial, the eletric field reduce in the silicon and increase in the buried oxide layer. The electric field in

buried oxide layer of BAGS is stronger than the conventional SOI, as the cut-line A of Fig.35 shown in Fig. 36. In Figs. 36, and 37, we can see the intersection of air and oxide will generate a protrusion of electric field in the middle of drift region. We will analyze the details of intersection electric field in the next part.This protrusion of electric field will disperse the high electric field at cathode side, see Fig. 38, the cut-line B in Fig. 35. Reduce the electric field in N^+ will result in a more uniform electric field and higher breakdown voltage. In this short sturcture, the shorter the length is, the greater effect will be. So, we proposed our sturcture.



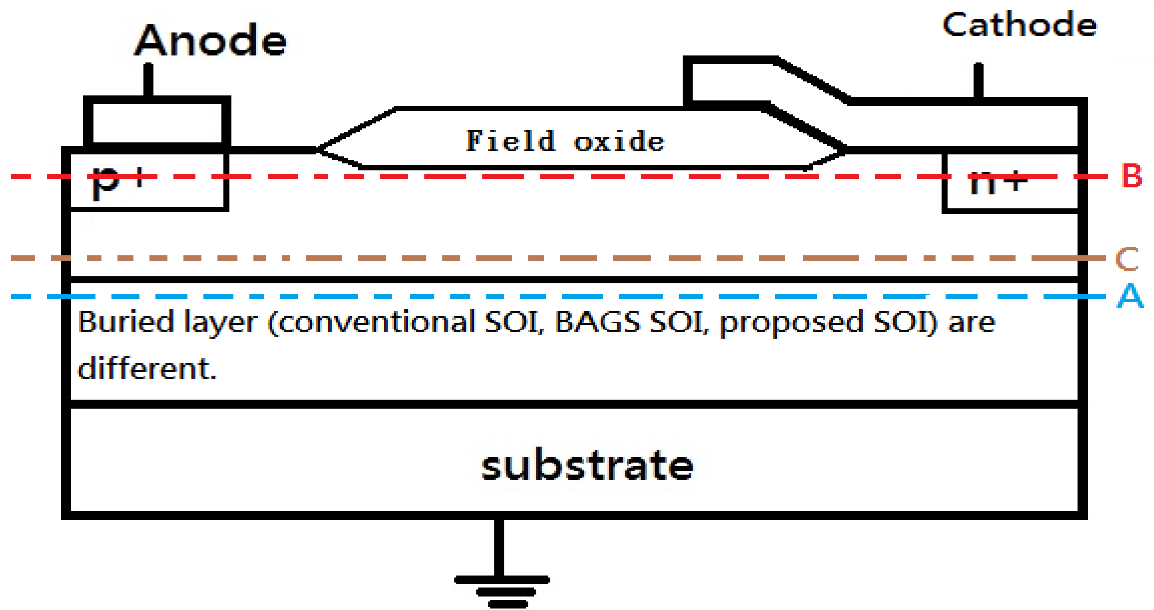


Fig. 35 The illustration of different cut-lines

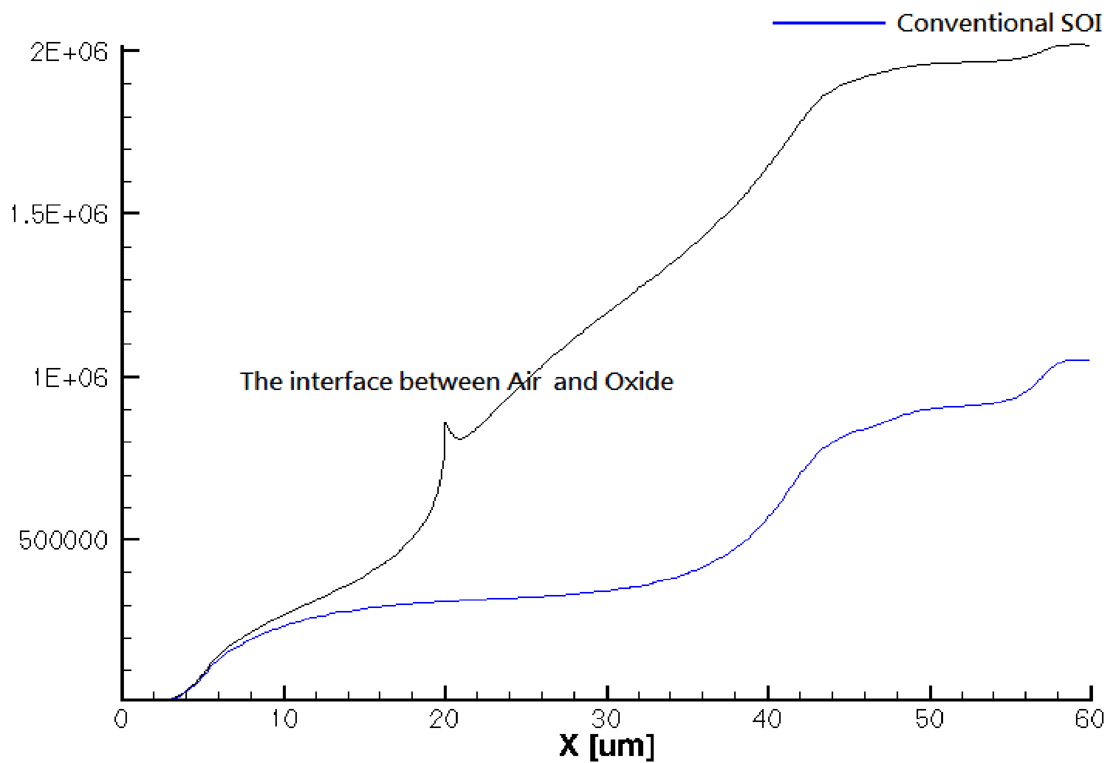


Fig.36 The buried oxide layer electric field for conventional SOI and BAGS SOI, cut-line A in Fig. 35

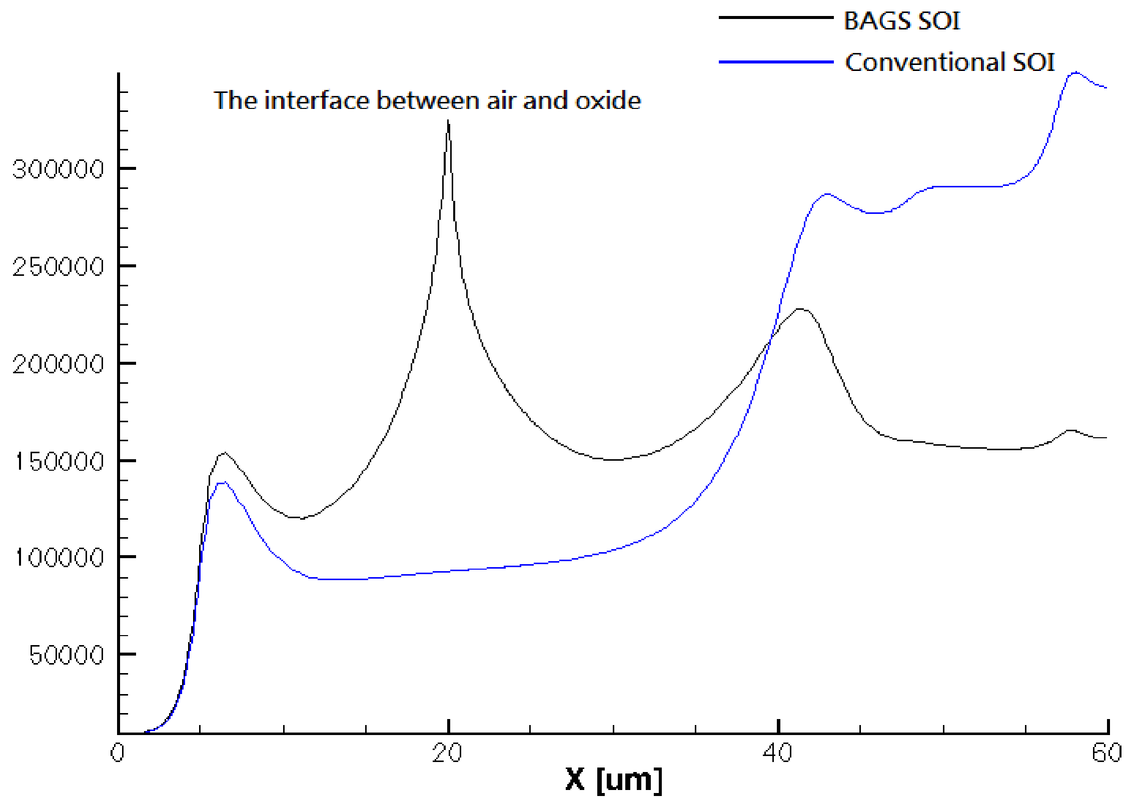


Fig.37 The silicon epi electric field for conventional SOI and BAGS SOI, cut-line C in Fig. 35.

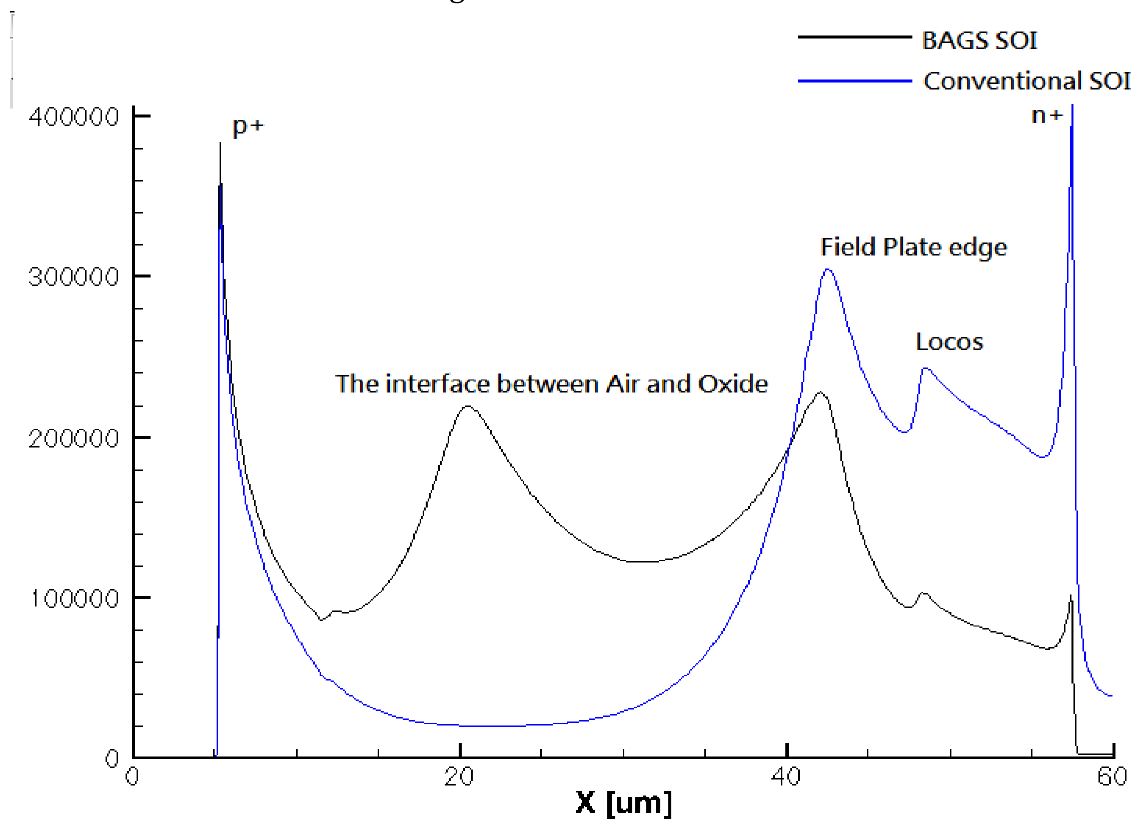


Fig.38 The surface electric field for conventional SOI and BAGS SOI, cut-line B in Fig. 35

Fig.39 is the electric field on the cut-line A, we can discover that the electric field is obviously jagged and cross following the patterned structure in the buried oxide layer of proposed structure. The whole electric field in the buried oxide layer is higher than BAGS. Fig.40 is the electric field on the cut-line C, like BAGS, there is a protrusion of electric field in the middle of drift region. However, the electric field under cathode side is higher than BAGS due to the patterned sturcture. The surface electric field, like the cut-line B of Fig. 35 is shown in Fig. 41. The electric field under the LOCOS and field plate are stronger than the BAGS. The whole electric field is more uniform.

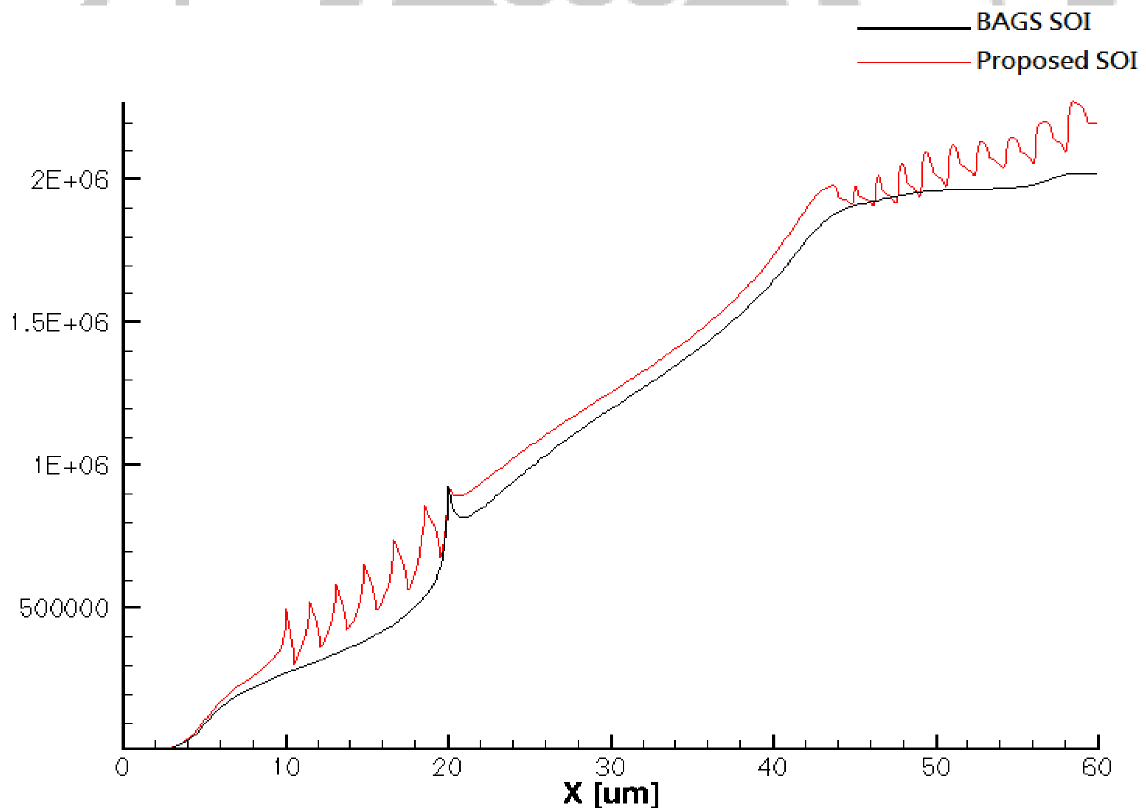


Fig.39 The buried oxide layer electric field for BAGS SOI and proposed SOI, cut-line A in Fig. 35.

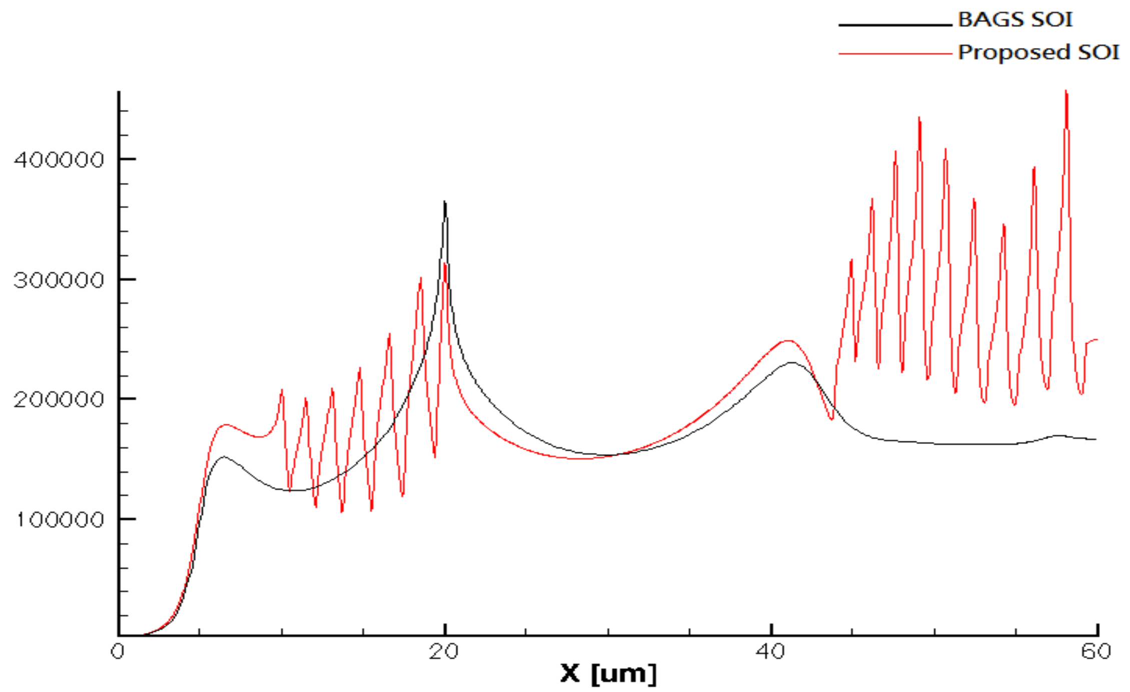


Fig.40 The silicon epi electric field for BAGS SOI and proposed SOI

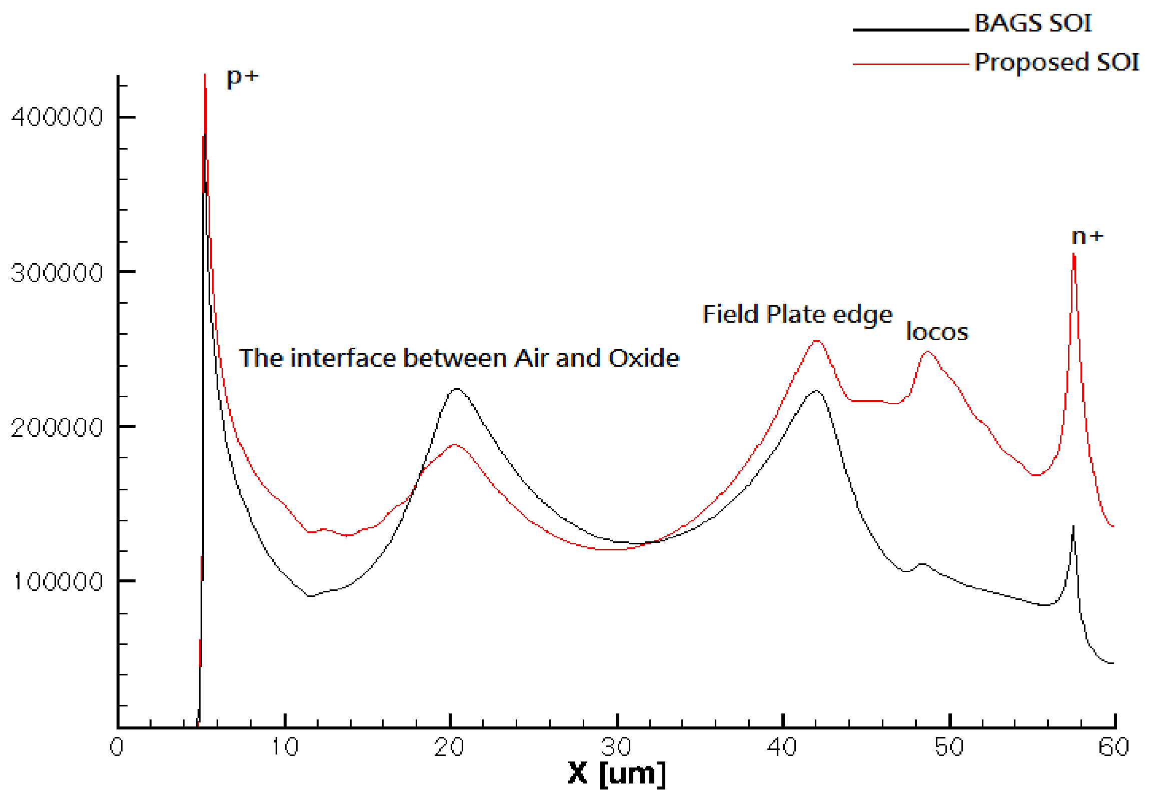


Fig. 41 The buried oxide layer electric field between BAGS SOI and proposed SOI, cut-line B in Fig. 35.

Fig. 42 below is the 3D electric field diagram. We can see the effect of electric field in buried layer to the inside of silicon layer. The circles are the electric field which needs to pay attention and the arrow point out the place which has been zoomed out in the circle. The electric field in the buried layer intersection of BAGS SOI affects the electric field in the silicon obviously.

Proposed SOI generates many protrusions of electric field by making multiple intersections of air and oxide. These protrusions of electric field obviously affect the electric field inside the silicn layer. The figure below have not analze the surface electric field yet. Fig. 43 is the 3D electric field diagram from silicon layer to surface electric field, as we can see most of the high electric fields were crowded at cathode and field plate edge. If the surface electric field is too strong, the device will breakdown realy. However, BAGS SOI and proposed SOI have electric fields which are generated by the intersections to make the electric field become more uniform. Due to the multiple intersections in proposed SOI, the surface electric field of proposed SOI is more uniform than BAGS SOI. Fig. 44 is the whole electric field of these three devices after overturning.

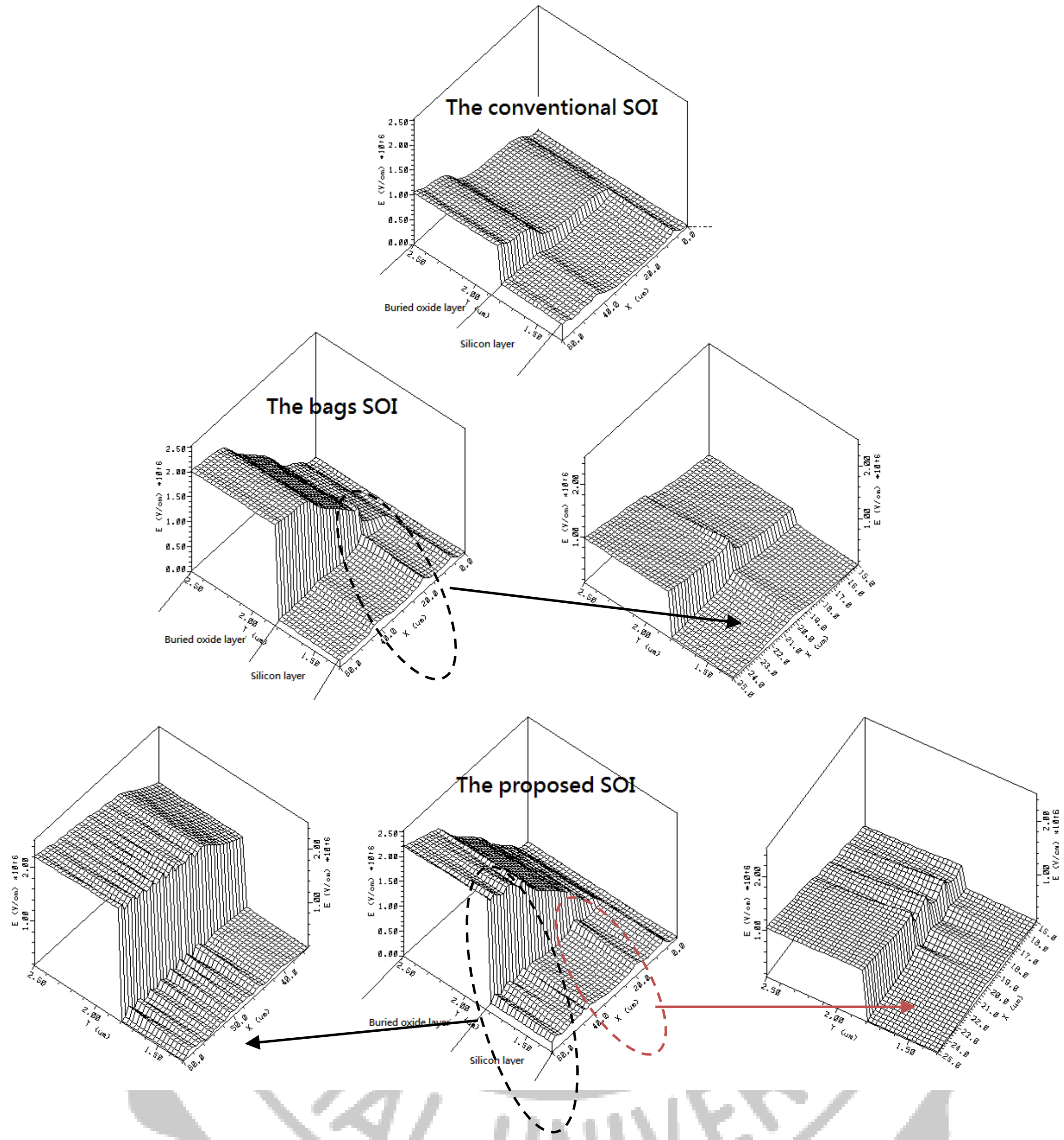


Fig. 42 3D electric field for silicon epi and buried oxide layer

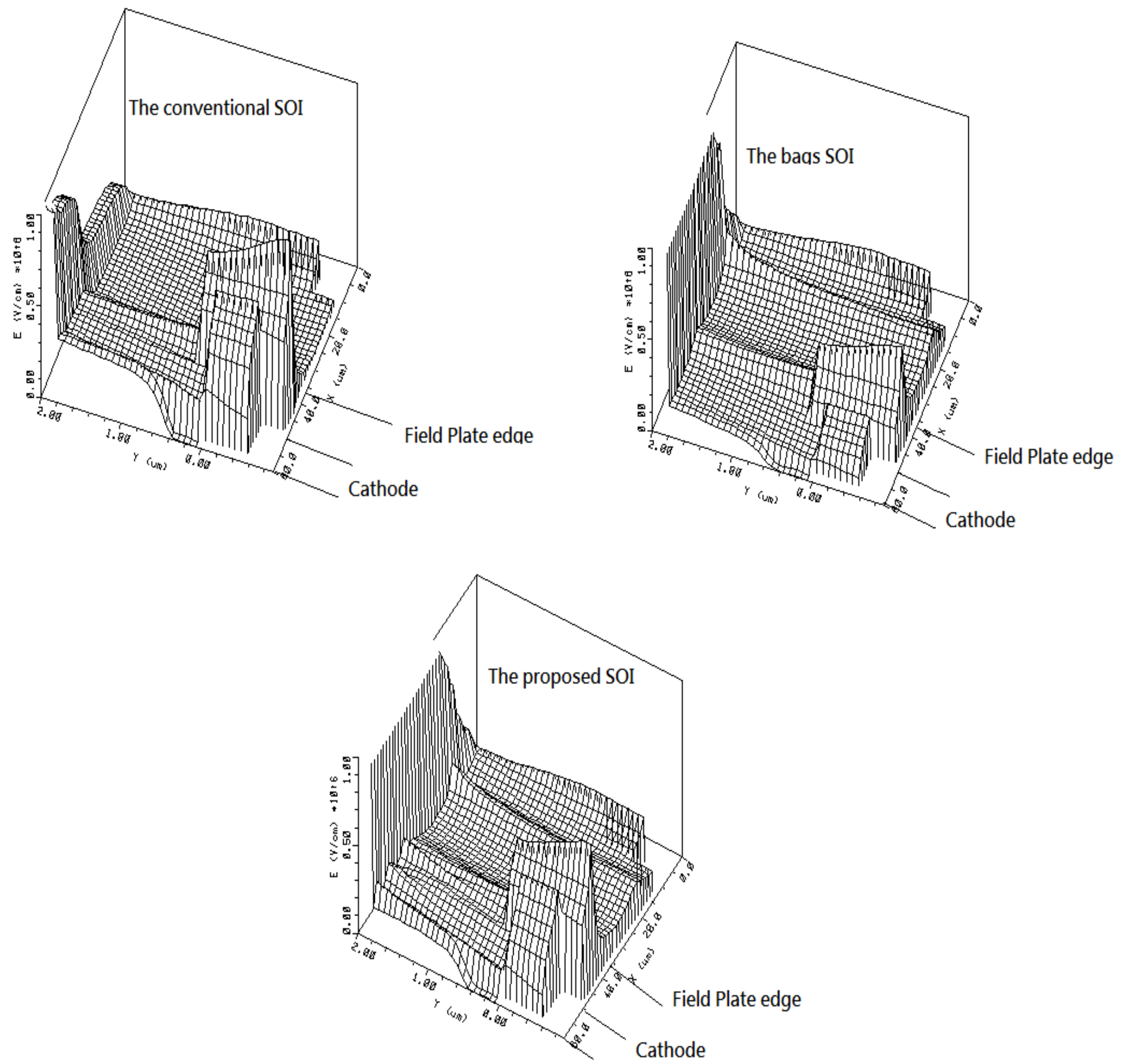


Fig. 43 3D electric field for silicon epi and surface.

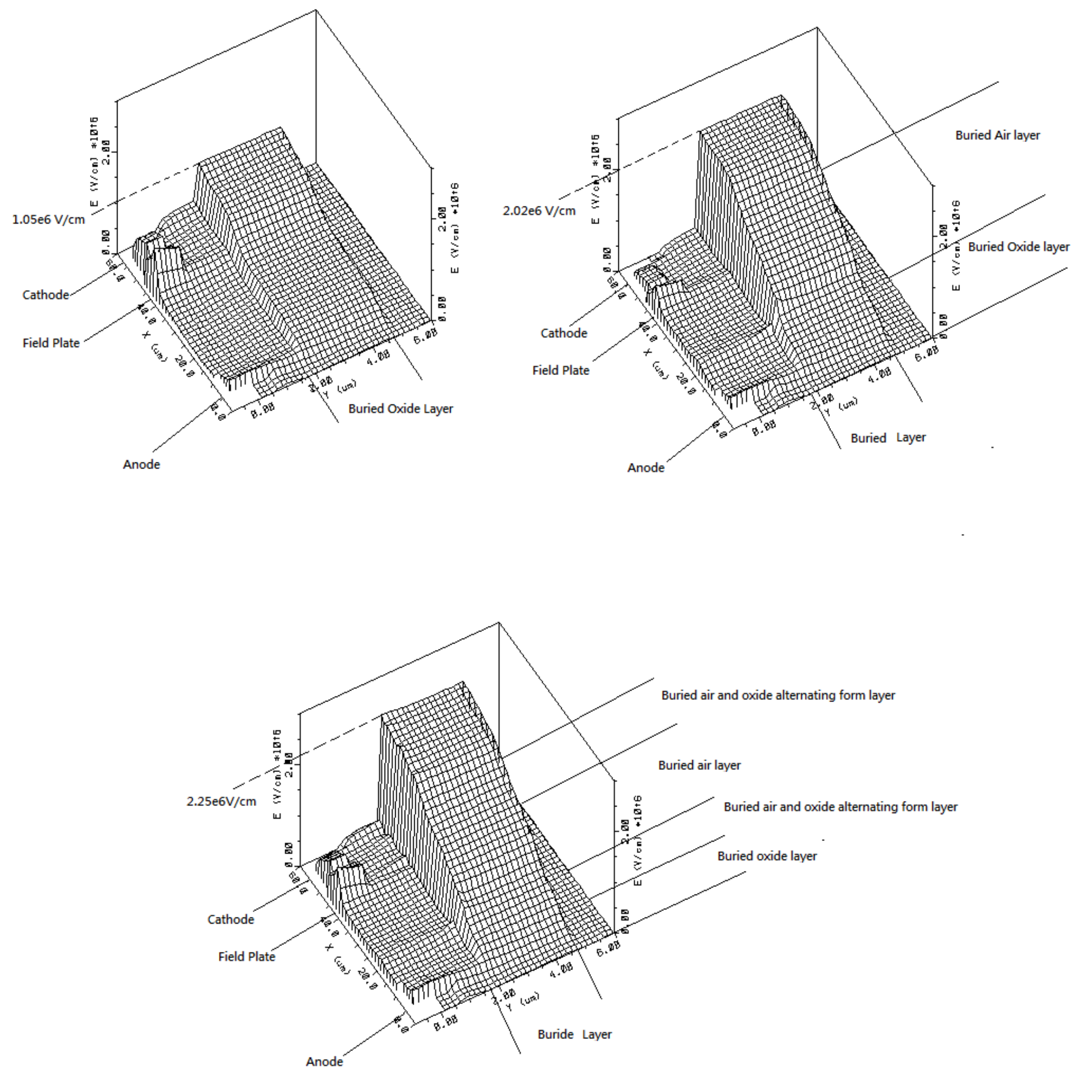


Fig. 44 3D electric field for all three types of SOI power devices

The location where breakdown occurs:

The surface electric field couldn't fully explain the situation of whole breakdown, that is why we need to analyze the impact ionization generation rate, called IIGR. We need IIGR to analyze the avalanche of our device when we not consider the punch through and Zener breakdown. As we can see from Fig. 45, the maximum IIGR of conventional SOI are crowded at cathode and field plate edge, makes it breakdown at cathode side early more easier. The maximum IIGR of BAGS SOI is crowded at the intersection between air and oxide. However, it pulls down the electric field at the field plate edge.The maximum IIGR of the proposed structure is crowded at field plate edge nearby the patterned structure at the anode side which makes the proposed SOI has the highest breakdown voltage.

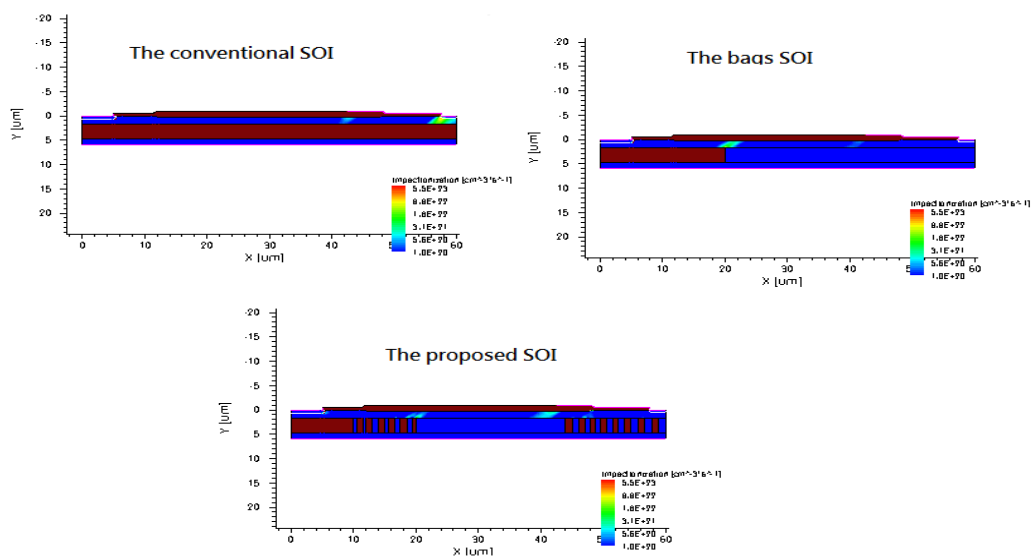


Fig.45 The maximum IIGR of three types of devices

4.5 Shorten the drift region length for lower on-resistance.

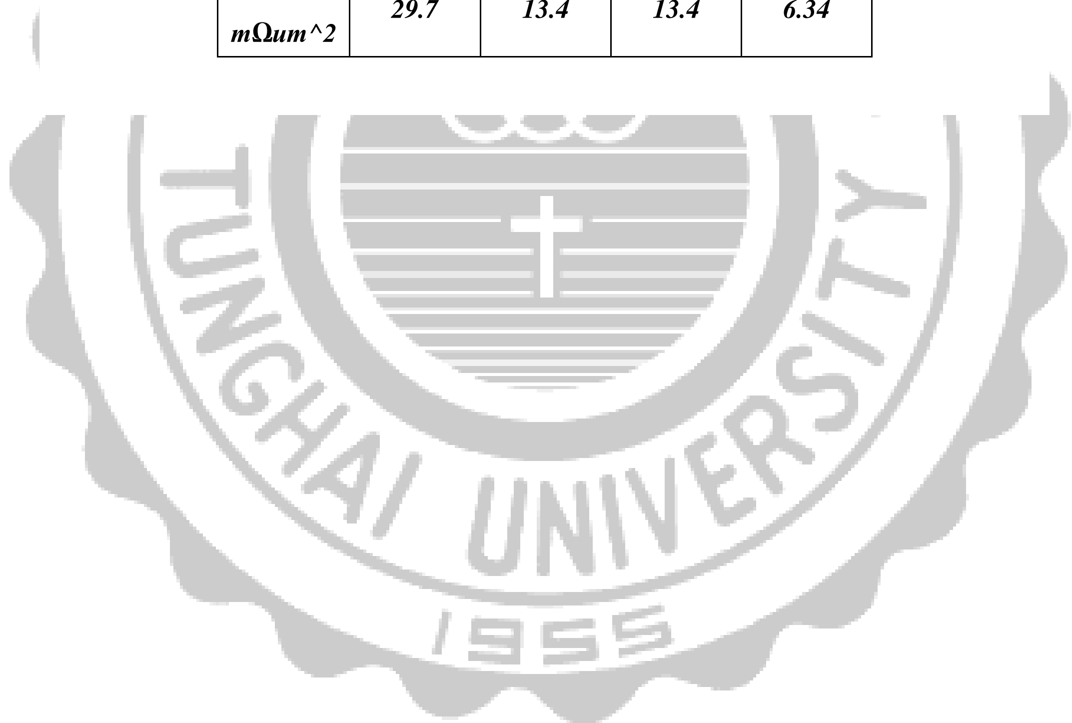
Table 2 shows that when the drift region is 80μm or 120μm, the breakdown voltage for conventional device is about 350-370V. BAGS devices indeed have much higher breakdown voltages, up to about 700V. And the breakdown voltage of our proposed device is a little bit higher than the BAGS one. When analyzing the turn-on properties, if the breakdown voltage is kept the same for these three devices discussed in this work, Table 3 shows that only the drift region length of the proposed structure can be reduced to make the R-ON lower. The corresponding turn on resistance is also given in Table2. For 680V and 620V, the length of our proposed device is 75% of BAGS, and the $R_{on,\ sp}$ is about 45 % to that of the BAGS.

Table. 2 Drift region length vs. breakdown voltage

BV/Device Length	*Conventional SOI*	*BAGS SOI*	*Proposed SOI*
60um	*351V*	*620V*	*680V*
80um	*368.3V*	*680.8V*	*720V*
120um	*367V*	*728V*	*757V*

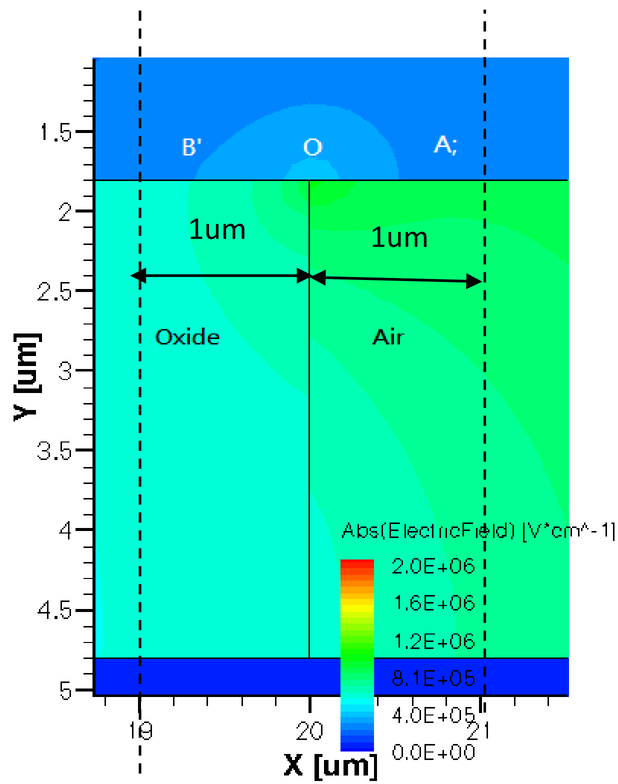
Table. 3 Drift region length vs. on-resistance

	BV=680V		***BV=620V***	
	BAGS SOI	***Proposed SOI***	***BAGS SOI***	***Proposed SOI***
Epi Layer Length	***80um***	***60um***	***60um***	***45um***
R-on (V*um/A)	***3.72*10^2***	***2.24*10^2***	***2.24*10^2***	***1.41*10^2***
R-on, sp mΩum^2	***29.7***	***13.4***	***13.4***	***6.34***

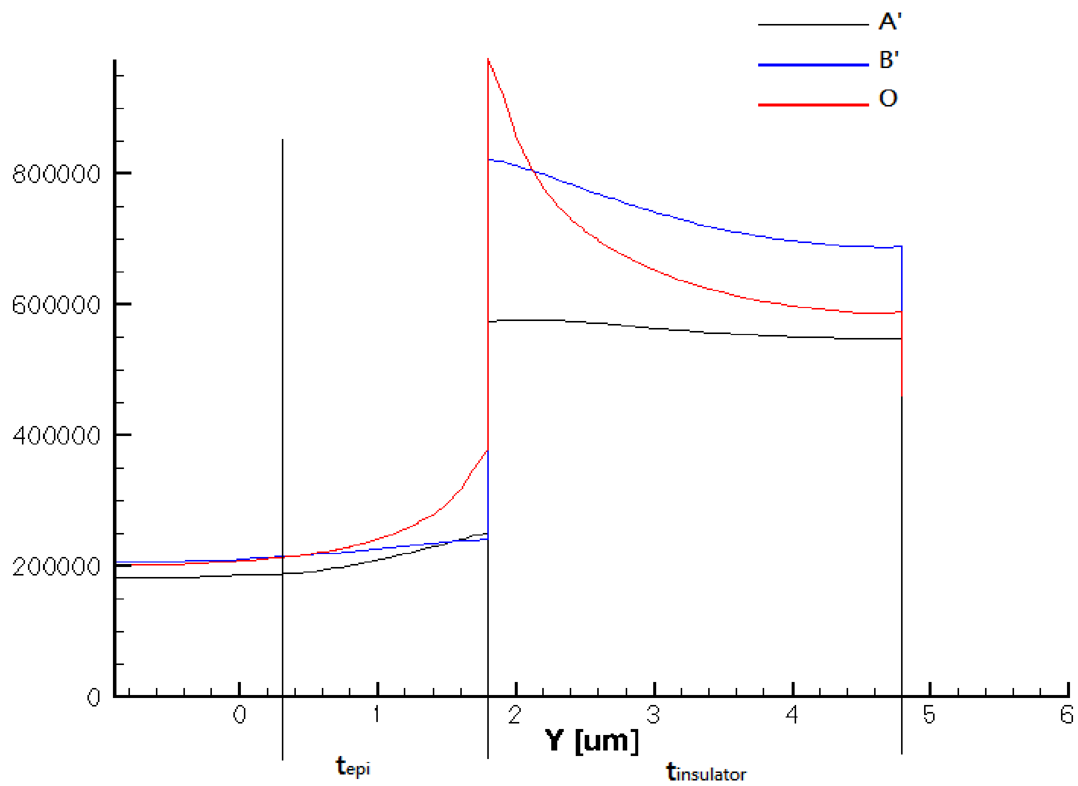


4.6 Analysis of patterned design

In this chapter, we discuss the design and the position of the pattern. As we know, the purpose of pattern design is to generate more electric field peaks at the intersection of air and oxide. First of all, we discuss the ratio of air to oxide which will affect the electric field. Point O in Fig. 46 is the intersection of air and oxide, and the cut-lines at points A and B show the electric fields in the oxide and air, respectively. We can tell from the electric field cut-line that inside the silicon epi, electric field (at point O)> electric field (at point A')> electric field (at point B'). The maximum electric field is located at the intersection, when the electric field of oxide and air decrease together, the electric field of oxide will decrease more than air. We can adjust the whole electric field of the device by putting multiple intersections.



(a)



(b)

Fig. 46 The analysis of vertical electric field at points A', B' and O, the black line at 0.3 μm is the silicon epi surface.

The relationship between dielectric width and electric field:

Here we fix the width of oxide to 1um, matching different width of air to discovering the deviation of electric field in intersection, as shown in Fig. 47. The 10 μm oxide is under the 5 μm anode, then we put air with width of 3 μm and 2 μm beside the oxide to make the gradient structure. The cut-line of the intersection of air and oxide (at y=1.8μm and x=10μm) is shown in Fig. 47(c), we can find that the intersection electric field is stronger when the width of air is 3 μm. From Fig. 48, we can tell that the electric field of 3 μm gradient device is crowded at the anode side. The drift region is not fully deplete yet, leads to the breakdown of the device is lower than the conventional SOI. In the 2 μm gradient device, the electric field is distributed around cathode side. In Fig. 49, the breakdown point was drift to the cathode side, due to the electric field of cathode side become stronger in the 3 μm device and the 2 μm one is the same as the conventional SOI.

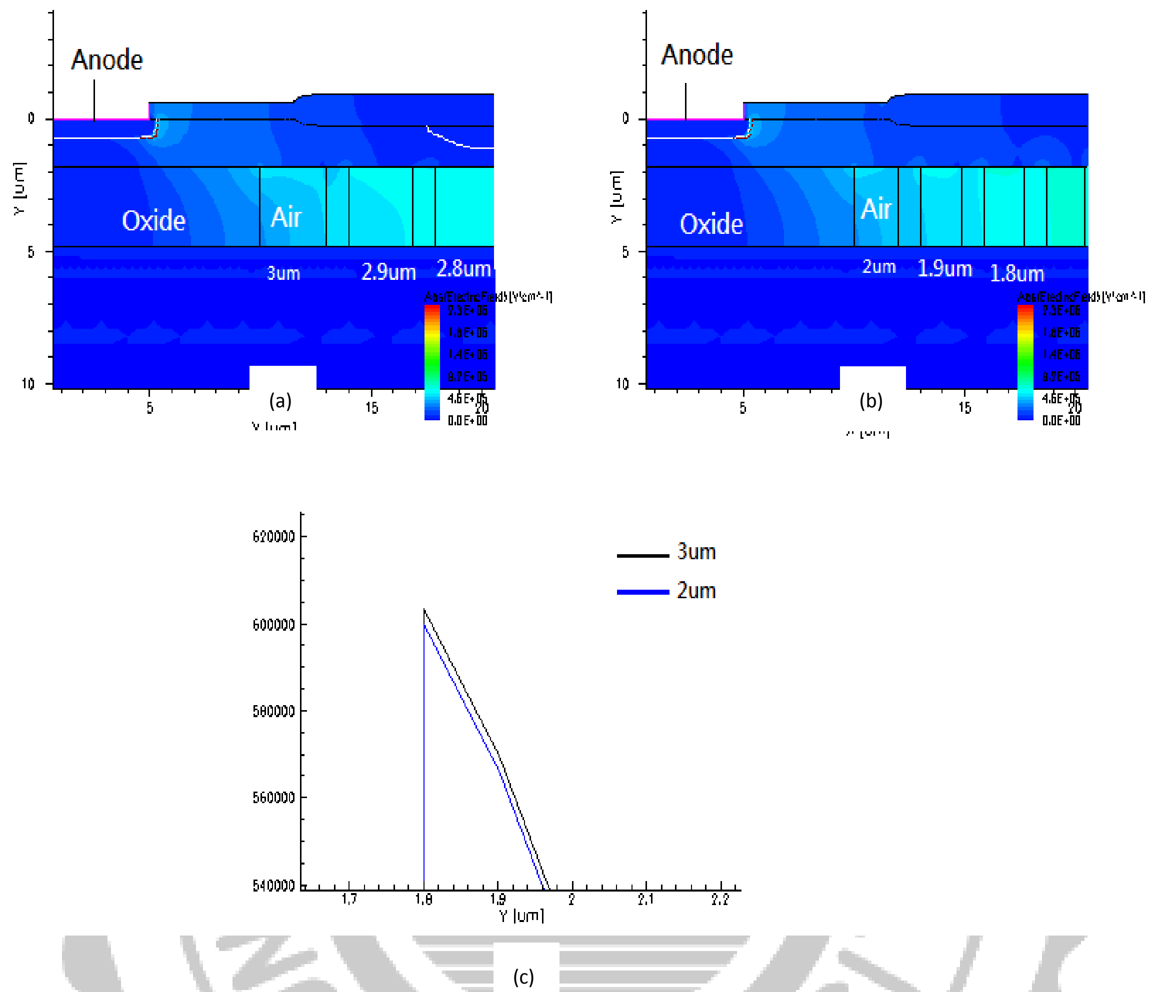


Fig. 47 Analysis of the dielectric width vs. electric field; (a) 3μm structure, (b) 2μm structure, (c) comparison of the vertical electric field.

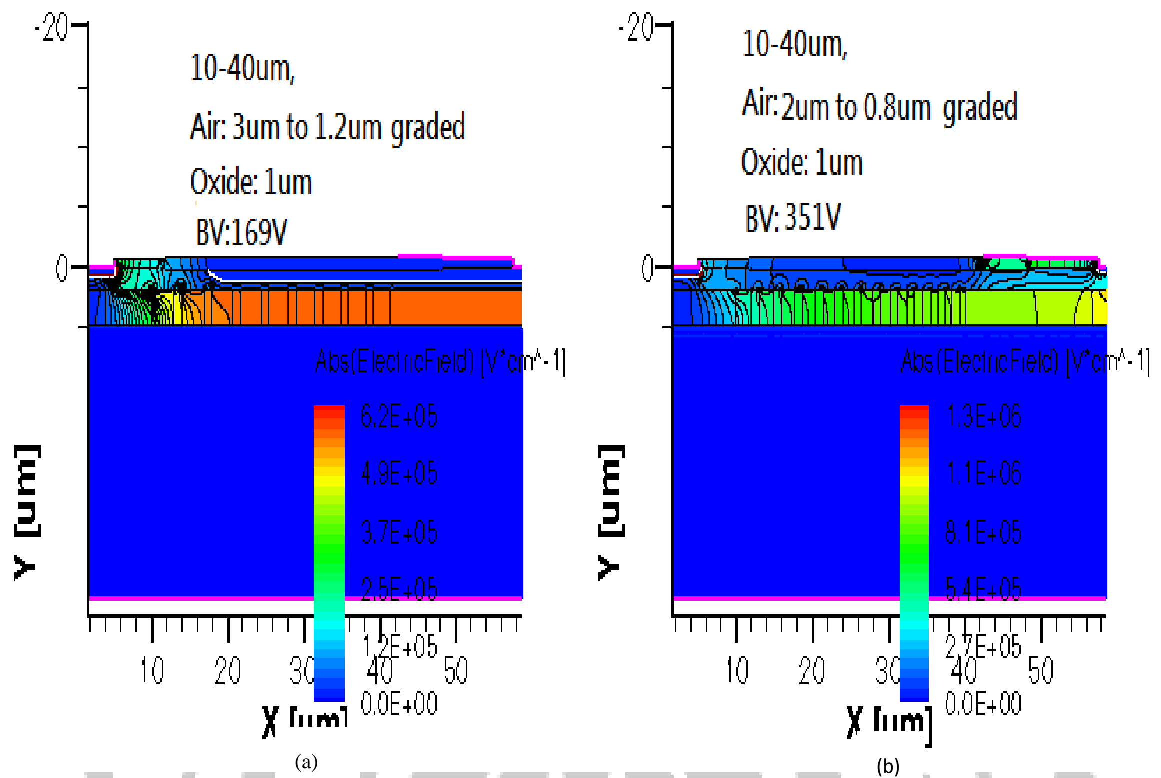


Fig.48 The electric field of (a)3μm graded SOI (b)2μm graded SOI

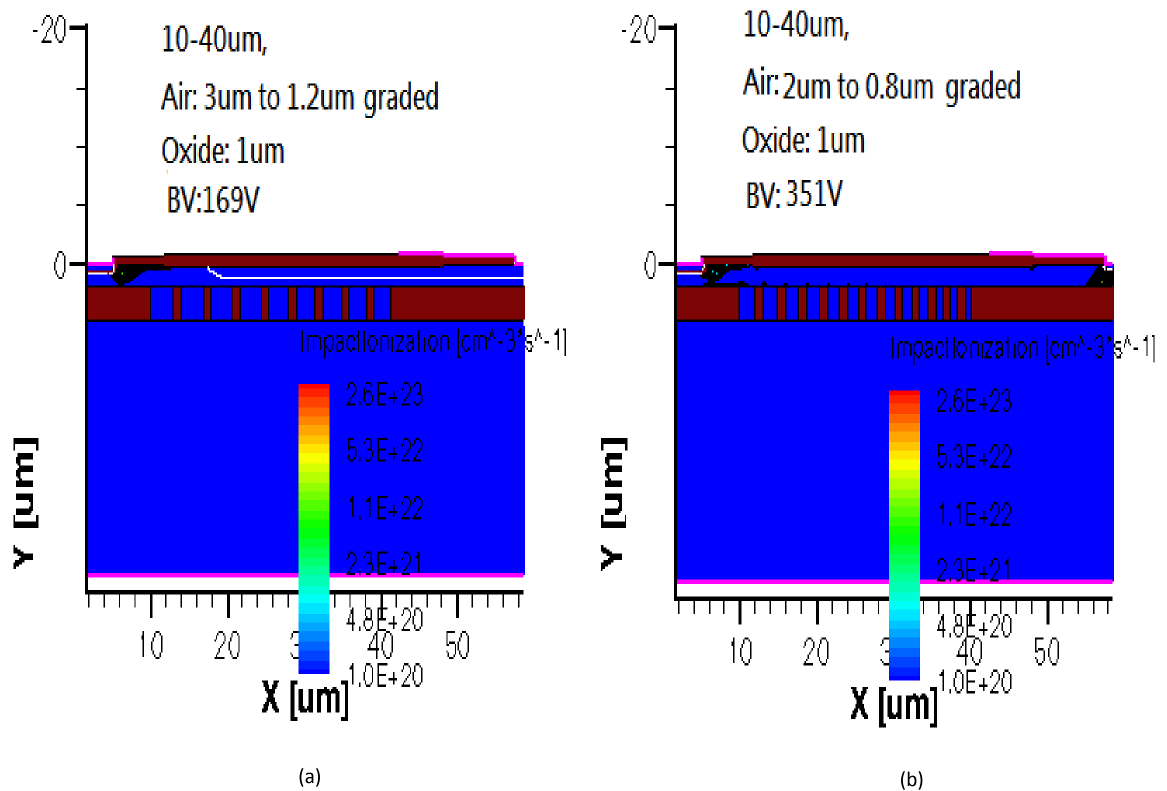


Fig.49 The maximum IIGR of (a) 3μm graded SOI (b)2μm graded SOI

We can reach some conclusions from the above analysis. This technique uses a layer of oxide with a sequence of slit openings for masking of the air in the buried oxide. Like the concentration of doping from heavy to light, the size of air area from large to small will affect the electric field from strong to weak.

BAGS structure only has one intersection, so the generated electric field will be too strong leads to locos and field plate out of action. The purpose of this thesis is to put the pattern design corresponds to field plate, locos, and the intersection of air and oxide in the BAGS. The arrows in Fig. 50 point out the stronger electric field we design. That is the air area which becomes wider and wider. Due to the field plate and locos, the electric field won't be push to under the cathode side.

Simulation results have shown that the new structure can provide higher breakdown voltages and lower turn-on resistance.

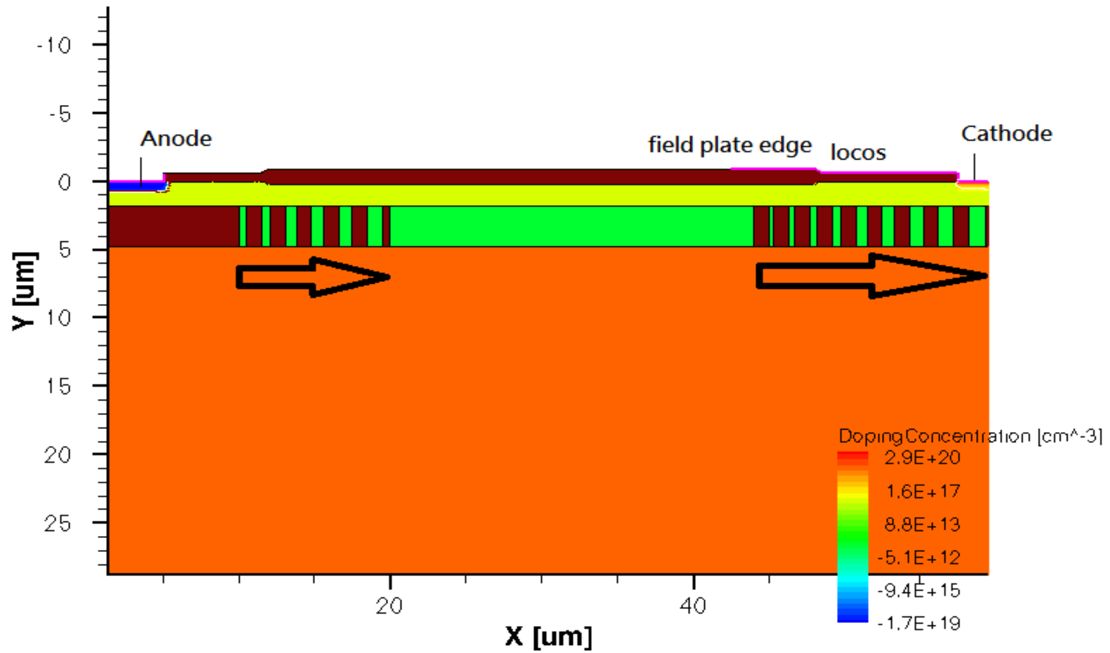


Fig.50 The enlarged drawing of proposed SOI

4.7 Results

The BAGS structure just only created a new peak electric field near the middle of drift region that pulls down the other peaks within the silicon layer, but the proposed structure has a uniform electric field that is similar to the linearly doped SOI. The length of air is wide the electric field is high, so we can set the gradient pattern based close to where we want. The purpose of this work is to propose a structure that increases the number of the electric field peaks, resulting in a more uniform electric field. For ultra-high voltage applications, as the length of the device drift region increases, the electric field difference between middle of the drift region and the ends of device increases. Therefore,

we need two patterned areas. The breakdown voltage for BAGS device is 620V, for proposed device is 680V; because the electric field is increased for the proposed device for more segments. Due to the concentration is unchanged, the turn-on resistances for these two devices are the same. To obtain the same breakdown voltage, the drift region of the proposed SOI can be decreased. The simulation result also shows that with the same breakdown voltage of 620V and 680V, the proposed SOI can make a shorter device. And we proposed a feasible process, the smart-cut technique. Before the wafer bonding process, the buried SiO_2 layer is selectively etched to obtain the proposed structure with air and oxide in an alternating form. The result will be like the previous electric filed diagram, the electric field becomes more uniform. The smart-cut technique is a common and can make wafer thinner process, so our structure that in buried oxide layer can affect the surface electric field. Not only don't affect the R-ON of silicon epitaxial, but the thinner high voltage device can combine with low voltage devices. Simulation results have shown that the new structure can provide higher breakdown voltages and lower turn-on resistance.

CHAPTER 5 Conclusions

This thesis proposed a new structure that is used in the buried oxide layer. Due to the structure is not in the silicon epitaxial layer, we can keep the breakdown voltage higher than 600V and to reduce the length of the device to decrease the R-on. We proposed the device in the smart-cut technique, because the smart-cut can make a thinner device to make our structure in the buried oxide layer and to affect the surface electric field .The thinner wafer process can help the low-voltage and high-voltage devices be put together in the same chip.

The pattern of our structure uses just only the etch process, so we can design the pattern to follow the other complex device. The SOI has ideal isolation, so we can use our structure to form LIGBT and LDMOSFET in the future.

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References

[1]S. D. Zhang, Johnny K. Sin, Tommy M. L. Lai, " *Numerical Modeling of Linear Doping Profiles for High-voltage Thin-film SO1 Devices*", IEEE Transactions on Electron Devices, vol. 46, no. 5, May 1999.,pp. 1036–1041,

[2]H. Zitta, "*Smart Power Circuits for Power Switches Including Diagnostic Functions*", Proc. of workshop AACD, Eindhoven, 1994.

[3] "*The Advantages of the Dielectric Isolation Process to the Application of High Voltage Integrated Circuits"*, http://www.dionics-usa.com/PDFs /Archives /Advantages %20of%20DI%20Process. pdf.

[4]Wolfgang Pribylm, "Integrated Smart Power Circuits Technology, Design and Application*"*..A-9500 Austria.

[5]J.M. Sun, F. Jiang, L.P. Guan, Z.B. Xiong, G.Z. Yan and J.K.O. Sin," *A New Isolation Technology for Automotive Power-Integrated-Circuit Applications"*, IEEE Transactions on Electron Devices, vol. 56, no. 9, September. 2009, pp. 2144–2149.

[6]T. K. H. Starke, P. M. Holland, S. Hussian, W. M. Jamal, P. A. Mawby, and P. M. Igic, ,"*Highly effective junction isolation structure for PICs based on standard CMOS process"*, IEEE Trans. Electron Devices, vol. 51, no. 7, , Jul. 2004, pp. 1178–1184

[7]Hardikar, S,Tadikonda, Green, D.W, Vershinin, K.V,Narayanan, E.M.S. "*Realizing high-voltage junction isolated LDMOS transistors with variation in lateral doping"*, Electron Devices, IEEE Transactions on, Volume: 51, Issue: 12, Dec. 2004,pp.2223 - 2228

[8]Oliver Triebl. " *Reliability Issues in High-Voltage Semiconductor Devices"*. http://www.iue.tuwien.ac.at/phd/triebl/node10.html

[9] "*P-N Junction Isolation"*, http://www.circuitstoday.com.

[10]A. Nakagawa , N. Yasuhara and Y. Baba , "*Breakdown voltage enhancement for devices on thin silicon layer/silicon dioxide film"*, IEEE Trans. Electron Devices, vol. 38, no. 7, 1991,pp.1650 -1654

[11]B. Zhang, Z Li, S Hu, X. Luoet al, " *Field enhancement for dielectric layer of high-voltage devices on Silicon on insulator"*, IEEE Trans. Electron Devices, vol. 56, (10), October 2009, pp. 2327 --- 2334.

[12]M. Chan, F. Assaderaghi, S. A. Parke, and C. Hu, "*Recessed-channel structure for fabricating ultrathin SOI MOSFET with low series resistance"*, IEEE Electron Device Lett., vol. 15, 1994 , p.22 -24

[13]S. Merchant, E. Arnold, H. Baumgart, S. Mukherjee, H.Pein, and R.Pinker,"*High-breakdown-voltage devices in ultra-thin SOI*", in Proc.IEEE SOI Conf., 1991, pp. 150–151.

[14]Hyoung-Woo Kim, Yearn-ik Choi, Sang-Koo Chung, "*Linearly-graded surface-doped SOI LDMOSFET with recessed source*",,Volumes 51–52, May 2000, pp. 547–554

[15]R.Sunkavalli,A.Tamba,B.J.Bbaliga. "*Step drift doping profile for high voltage DI lateral power device*",IEEE international SOI Conference, Oct 1995, pp.139 - 140

[16]許健,楊紹明,"利用垂直線性摻雜飄移區發展 SOI 元件",亞洲大學,碩士論文

[17]許健,劉彥伶,曹世昌,"超薄型(0.15 微米)SOI LDMOS 高壓(>800V)元件之研究",亞洲大學,碩士論文

[18]S. Yang, W. Tseng, and G. Sheu, "*Dependence of Breakdown Voltage on Drift Length and Linear Doping Gradients in SOI RESURF LDMOS Devices*" ,9th International Conference on Electronic Measurement & Instruments, 2009 (ICEMI'09), pp. 4-594 – 4-597

[19]Jeon BC, Kin DY, Lee YS, *"Buried air gap Structure for improving the breakdown voltage of SOI power MOSFET's*.",Proceedings of the PEMC; 2000. p. 1061–63.

[20]Xiaorong Luo, , Bo Zhang, Zhaoji Li, "*A new structure and its analytical model for the electric field and breakdown voltage of SOI high voltage device with variable-k dielectric buried layer*",Volume 51, Issue 3, March 2007, Pages 493–499

[21] WP. MasZara.,"*Silicon—On—Insulator By Wafer Bonding and Etch—Back*",IEEE SOS/SOI Technology Work shop, (Oct. 1988), 1 pg

[22]K. Thompson, "*Direct silicon-silicon bonding by electromagnetic induction heating*", J. Microelectromech. Syst. 11,2002, p.285-9

[23]K.Sakaguchi, K.Yanagita, H.Kuris, H.Suzuki, K.Ohmi and T.Yonehara, "*ELTRAN® by Splitting Porous Si Layers*", Proc.9th Int. Symp.on Silicon on Insulator Tech. and Devices, vol.99-3, The Electrochemical Society, Seattle, (1999), pp.117-121,

[24] T. Yonehara and K. Sakaguchi, "*ELTRAN; Novel SOI Wafer Technology*,"JSAP,no.4, 2001.

[25]Atsuki Matsumura, Keisuke Kawamura, Yoichi Nagatake, Seiji Takayama,US Pant NO.US7067402

[26]Andrew Wittkower, Andre Auberton-Hewe and Christophe Maleville , "*SM ART-CUT@ Techno logy for : A new high volume application for ion implantation*",Ion Implantation Technology, 2000,pp.269 - 272

[27]Joy Johnson, "*Hydrogen Ion-Implantation in SmartCut® SOI. FabricationTechnique* ",http://http://web.mit.edu/joyj/www/Projects_files/6.774%20Final%20Project%20Report.pdf.

[28]SOITEC,http://http://www.soitec.com

[29]S. Merchant, E Arnold, H Baumgon., "*Realization of high breakdown voltage (>700 V) in thin SO1 devices*", *Proceedings of ihe 3rd International Symposium on Power Semiconductor Devices and ICs*", Baltimore, MD, USA, Apr 22-24 I991, pp.3 1 - 35

[30]F. Udrea, D. Gamer, K. Sheng, "*SO1 Power Devices, Electronics & Communication Engineering Journal*", 2000, 12, pp.27-40.

[31] S. Merchant, E. Arnold, H. Baumgart, R. Egloff, T. Letavic, S.Mukherjee, and H. Pein, "*Dependence of breakdown voltage on drift length and buried oxide thickness in SOI RESURF LDMOS transistors*" ,in ISPSD Tech. Dig., 1993, pp. 124–128.

[32]潘俊廷,"SOI 功率元件分析",逢甲大學,國家圖書館

[33]Xiaorong Luo，Zhaoji Li，"基于介质电场增强理论的 SOI 横向高压器件与耐压模型-緒論", University of Electronic Science and Technology of China,博士論文

[34]R.P.Zingg, I.Weijland, H.V.Zwol,"*850V DMOS-switch in silicon-on insulator with specific Ron 13Ω-mm^2*", IEEE International SOI Conference. Proceedings, 2007, pp.62

[35]I. J. Kim, S. Matsumoto, T. Sakai, and T. Yachi, "*Breakdown voltage improvement for thin-film SOI power MOSFET's by a buried oxidestep structure*," IEEE Electron Device Lett., vol. 15, no. 5, May 1994 ,pp. 148–150,

[36]BaoxingDuan, Bo Zhang, and ZhaojiLi, "*New Thin-Film Power MOSFETs With a Buried Oxide Double Step Structure*",IEEE ELECTRON DEVICE LETTERS, VOL. 27, NO. 5, MAY 2006

[37]F. Udrea ,"*Ultra-fast LIGBTs and superjunction devices in membrane technology*", Proc of ISPSD 2005, pp-267-270.

[38]T. Trajkovic, F. Udrea, C. Lee, N. Udugampola, V. Pathirana, A. Mihaila, and G. A. J. Amaratunga, "*Thick silicon membrane technology for reliableand high performance operation of high voltage LIGBTs in Power ICs*," in Proc. Int. Symp. Power Semiconduct. Devices IC's, 2008, pp. 327–330

[39]A,Nakagawa,N.Yasuhara,Y.Baba, "*Breakdown Voltage Enhancement for Device on Thin Silicon Layer/ Silicon Dioxide Film*", IEEE Transactions on Electron Devices,2002,pp. 1650 - 1654

[40]Baoxing Duan, Bo Zhang, Zhaoji Li, "*New thin-film power MOSFETS with a buried oxide double step structure*", IEEE Electron Device Letters, vol.27, pp. 377, 2006.

[41]罗小蓉,李肇基,张波,郭宇锋,唐新伟,"屏蔽槽 SOI 高压器件新结构和耐压机理 *" 半导体学报 2005

[42]P. RATNAM," *Novel silicon-on-insulator for high voltage for high-voltage integrated mosfet circuits*",Electronics Letter,1898,pp.536-537

[43]Udrea F, Popescu A and Milne W., *"Breakdown analysis in JI, SOI and partial SOI power structures* , "IEEE international SOI Conference, 1997.,p102- 130,

[44]Bart Van Zeghbroeck ,"*Principles of Semiconductor Devices* ",2011

[45]R. Victor Jones, "*Electronic Devices and Circuits Engineering Sciences 154*",http://http://people.seas.harvard.edu/~jones/es154/lectures/lecture_2/breakdown/breakdown.html. 2001

[46]John Wiley &SoncInc, "*Semiconductor Device Physic and Technology*",1997

[47]H. Iwamoto, H. Haruguchi, Y. Tomomatsu, J. F Donlon, and E. R. Motto,“*A new punchthrough IGBT having a new N-buffer layer*,” in Proc.
IEEE IAS, 1999, pp. 692–699.
[48]J. F. Donlon, E.R. Motto, K. Ishii, T. Iida, “*Application advantages of high voltage high current IGBTs with punch through technology*, ” in Conf. Rec. of IEEE Industry Applications Annual Meeting, Oct. 1997, pp. 955-960.
[49]Hung, Chun-yi, “以光罩佈局產生多維電場對半導體高壓元件的影響”,清華大學,碩士論文
[50]Huang, Jian-Fu “SOI 功率電晶體之模擬與特性分析”，清華大學，碩士論文