東海大學電機工程學系

碩士論文

乙太網路連接器降低串音之研究設計

A STUDY ON REDUCING CROSSTALK FOR A ETHERNET CONNECTOR

研究生：林博偉

指導教授：陳家豪 博士

中華民國 九十八 年 六 月

乙太網路連接器降低串音之研究設計

A STUDY ON REDUCING CROSSTALK FOR A ETHERNET CONNECTOR

研 究 生：林博偉　　Student：Bo-Wei Lin

指導教授：陳家豪 博士　　Advisor：Dr. Ja-Hao Chen

東海大學

電機工程學系

碩士論文

Department of Electrical Engineering

Tunghai University

Taichung, Taiwan, R.O.C.

Thesis for Master of Science

June, 2009

中華民國 九十八 年 六 月

東海大學電機工程學系碩士學位

考試委員審定書

電機工程學系研究所 林博偉 君所提之論文

中文：乙太網路連接器降低串音之研究設計

英文：A STUDY ON REDUCING CROSSTALK FOR A ETHERNET CONNECTOR

經本考試委員會審查，符合碩士資格標準。

學位考試委員會 召集人：蔡榮宏 (簽章)

委 員：

中 華 民 國 98 年 07 月 21 日

乙太網路連接器降低串音之研究設計

研究生 ： 林博偉　　指導教授 ： 陳家豪 博士

東 海 大 學 電 機 工 程 研 究 所

摘 要

本論文利用 ADS 2006A 作為電路模擬與電容設計之環境，並與實際量測結果比較，評估 RJ45 中 PCB 板傳輸線的效應。利用 ADS 電磁模擬的環境建構出所想要的傳輸線結構，再由實測驗證，由實驗資料發現 RJ45 轉接頭存在之寄生電容與寄生電感將造成傳輸線之訊號不匹配，並於 PCB 板中產生串音現象，進而降低傳輸品質。爲了滿足 CAT6 之規範，本研究利用指叉狀電容對傳輸線做補償，產生大小相等方向相反之差動訊號，讓每對傳輸線之訊號達到平衡，以降低寄生效應所產生之串音現象。研究中發現設計之電容模擬結果與實測之容值相符合，即可利用模擬環境精確的算出 PCB 板上電容之電容值，幫助建立補償電容。此外，設計接頭內部 PCB 板上之傳輸線，並由設計之成品完成傳輸線模擬環境之建立。過去對於降低串音訊號補償之方法並無一定之準則，大多採取試誤法，極為費時，又隨著頻率越來越高，寄生效應之影響對於補償電容之計算更為顯著，計算更為不易，故在此建立之模擬方法將可提高乙太網路接頭設計之效率。

A STUDY ON REDUCING CROSSTALK FOR A ETHERNET CONNECTOR

Student : Bo-Wei Lin Advisor : Dr. Ja-Hao Chen

Institute of Electrical Engineering
Tung Hai University

ABSTRACT

In this thesis the ADS2006A is used for designing and evaluating the effect on the PCB in RJ45 jack. The simulation environment can be used for designing the transmission line and be verified from the result of measurement and simulation. The parasitic capacitance and parasitic inductance in RJ45 Jack will cause the signal unbalancing and will occur the crosstalk which decreases the performance of transmission. In order to conform the specification of CAT6, the comb capacitor is used for compensating, which is result in the balancing signal for the reducing of crosstalk caused by parasitic effect. The simulation and measurement data of the capacitor we designed are compliant. Consequently, the simulation environment can be used for calculating and compensating the capacitance on PCB. Therefore, we also design the transmission line on PCB and build the simulation environment from the products. In the past, the method of reducing crosstalk in rj45 jack is trial- and –error and it is difficult and time-consuming. With the higher frequency, the influence of the parasitic effect is apparent and the calculation is more difficult. The method that we present in the thesis will increase the efficiency of designing the high speed Ethernet connector.

ACKNOWLEDGMENTS

I offer thanks to Dr. Ja-Hao Chen for suggesting the topic of this research. His prior insight and thoughts in the research was invaluable to me. He recommended and corrected my research work in the weekly meeting. I would like to acknowledge the oral examination commissioner Dr. Rung-Yu Tsai, Dr. Wei Liang Lin and Dr. Je-Hung Lin for providing renew suggestions in the thesis edition. I also wish to express my sincere appreciation to my partner, Shih Hsiang Liao and Cheng Lun Chu. Without the support of these professors this thesis would not have its present form. Finally, special thank are due to my parents for their moral and financial support for my education.

CONTENTS

TABLE OF CONTENTS

ILLUSTRATION OF CONTENTS

CHAPTER 1

INTRODUCTION

In recent years, the communication system is developed and the methods of communication are divided into two type: wireless and wire. The wire communication is particularly applied to the network because of the higher speed and capacity. The media of wire communication system is the transmission line which is used widely for the signal transmission. Transmission line has two forms, one is dual conductors like coaxial cable, microstrip line, twisted line, and the other is single transmission line like waveguide. The function of transmission line is to transmit signal from transceiver to receiver, and it causes the loss, that the strength of electromagnetic signal becomes small result from signal delivery and the parasitic effect between the transmission line. In order to satisfy specification of the high speed network, the improvement of the transmission line is very important. Recently, the purpose is to cancel the noise from the transmission path, and keep the data source complete. RJ45 is a modular connector conformed to the specification of Ethernet, and uses the unshielded twist pair (UTP) to deliver the differential signal that the high speed network is based on. Theoretically, a differential signal referred to as the ‘common-mode’, on the other hand, is carried

on two conductors, however the signal value is the difference between the individual voltages on each conductor, the average of the two voltages will often remain the same. The benefits of differential signal is that smaller DC signals can be easily discriminated and is highly immune to outside electromagnetic interference (EMI) and crosstalk from nearby signal conductors. Practically, the signal will not be balanced completely because of the parasitic effect from the component and material of transmission line and connector. The crosstalk in the UTP is usually caused by the untwisted end part of the cables in order for the twisted cables to be connected to the Modular Jacks. To compensate the unbalanced coupling capacitance is the method to reduce the crosstalk but it is too difficult to analyze and count accurately. In this thesis we demonstrate that using the EDA tool to assist in analyzing the influence of near end crosstalk for RJ45 connector and compensating the capacitor embedded PCB to conform the EIA/TIA standard. There are four chapters in this thesis. It will present the method that reducing the crosstalk noise in modular jack, to introduce the "CAT *6*" high speed data transmission modular jack, fundamental of crosstalk, and the method to balance the capacitive coupled crosstalk noise in second chapter. For third chapter, we design the comb capacitor embedded on PCB in RJ45 jack for balancing and design the transmission line embedded on PCB, and use EDA tool to establish the

simulation environment for analyzing and balancing the crosstalk noise. In fourth chapter, we test and verify the simulation environment and show the simulation and measurement result fitting the specification of Category 6. The final chapter will make a conclusion regarding this thesis.

CHAPTER 2

THE METHOD OF REDUCING CROSSTALK NOISE IN MODULAR JACK

2.1 Introduction

In recent year, the development of high-speed internet is more complete. With the increase of working frequency, the crosstalk noise has become a significant problem. In this chapter, we introduce the modular jack and the crosstalk reducing method, satisfying the CAT-6 specification for frequencies up to 250 MHz. CAT6 cable is an Ethernet cable standard defined by EIA/TIA (Electronic Industries Association and Telecommunications Industry Association), and more reliable for Gigabit Ethernet, which speed is up to 1Gbps. The high-speed operation of CAT-6 cable is based on differential mode signal transmission using unshielded twist pair (UTP) cable. The crosstalk characteristics of the modular jack on the printed circuit board (PCB) were improved by inserting embedded capacitors, which compensate for the unbalanced capacitive crosstalk in the plug and insert. Particularly, due to limit PCB area, the balancing capacitor is designed, with using a double-sided PCB design. Less than -46 dB connecting hardware NEXT loss was achieved after the crosstalk noise compensation, to satisfy the CAT-6 specification for frequencies up to 250 MHz.

2.2 The Modular Jack for High-Speed Ethernet

The modular jack used as Ethernet connector is typically called 8p8c (8 Position 8 Contact) connector or RJ45 connector. The RJ45 connector has two main components: the male plug and the female socket with eight channels. The conductors on the male plug are flat, and the conductors inside the socket are suspended diagonally. The modular jack consists of four pairs of twisted wires, the plug, socket shell, the insert, and PCB. The majority of the crosstalk noise is generated in the untwisted region of the wires in the plug and insert.

.

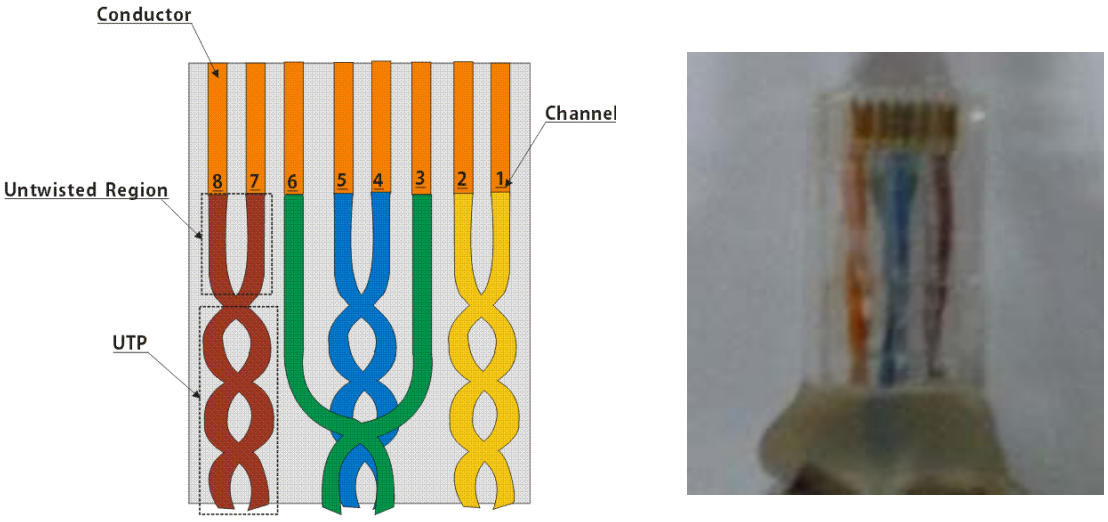


Fig.2.1.1 The plug of CAT-6 has an untwisted region, resulting in crosstalk noise between nearby pairs at the 250 MHz operational frequency of the CAT-6 network systems.

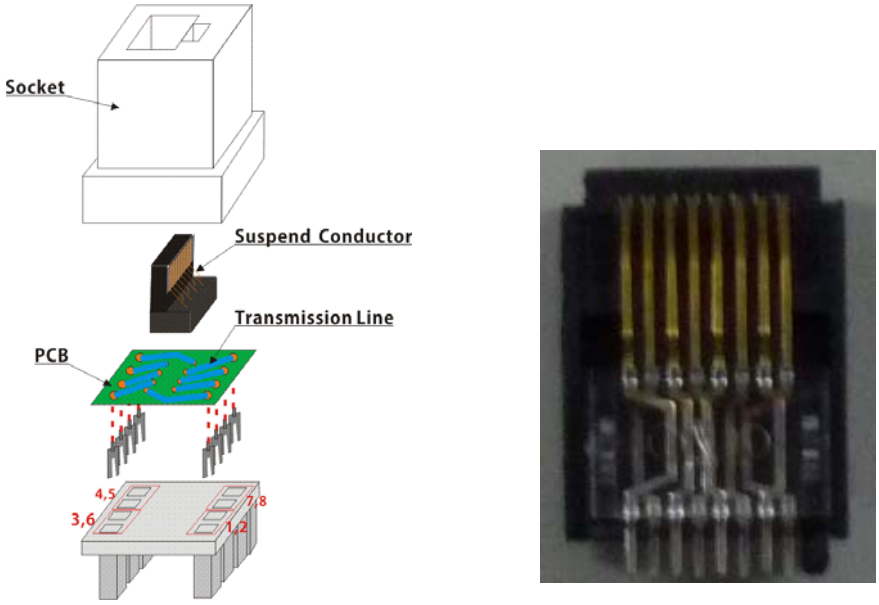


Fig.2.2 The modular jack consists of four pairs of twisted wires, the plug, the housing, the insert, PCB, and IDC.

The cable will be “untwisted” when the contact between plug and the insert to conform the specification of network transmission. Therefore, the influence of the capacitive coupling must be minimized to reduce the crosstalk noise. But the mutual capacitances cannot be removed because the natural phenomenon. The available method is to cancel them by adding balanced capacitive crosstalk in the modular jack. We can add mutual capacitance on the PCB inside the modular jack for the purpose of balance.

2.3 The Foundation of Crosstalk

Crosstalk is caused by the mutual inductance and mutual conductance, which is result from two nearby transmission line. In particular, the higher density of the circuit layout on PCB, the problem of crosstalk is more serious. A crosstalk can be divided into three group, crosstalk through common impedance, inductive crosstalk, and capacitive crosstalk. The capacitive crosstalk is universal in the high frequency application. And crosstalk also can be divided into two classes: far end crosstalk (FEXT) and near end crosstalk (NEXT).

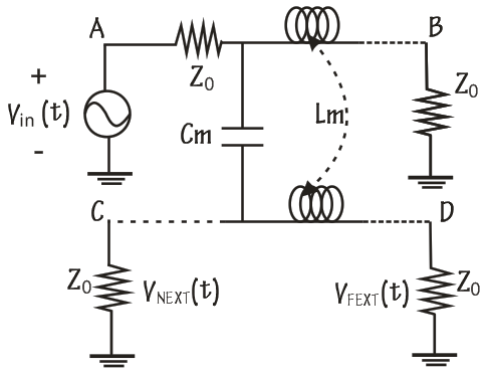
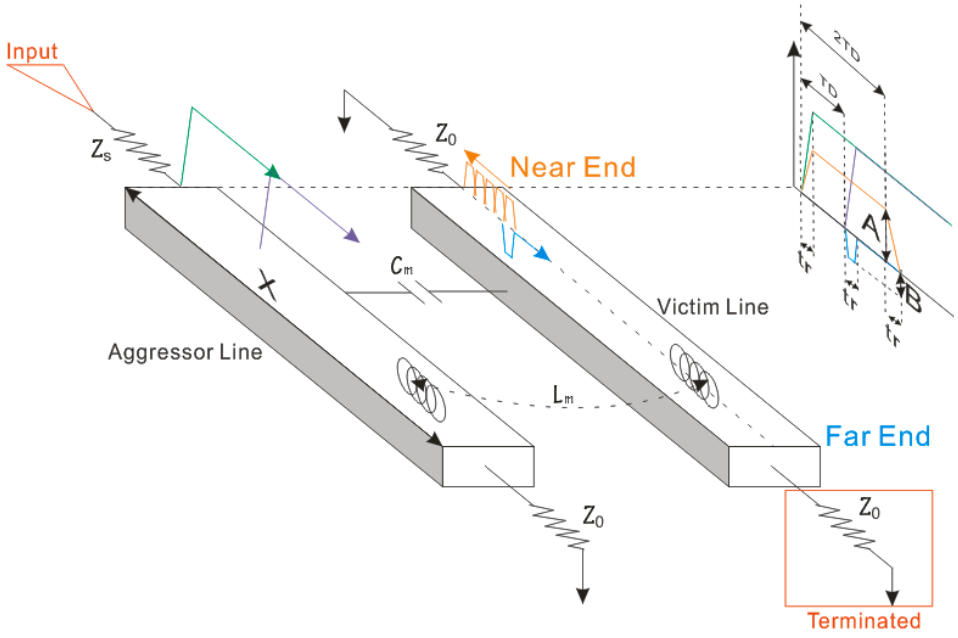
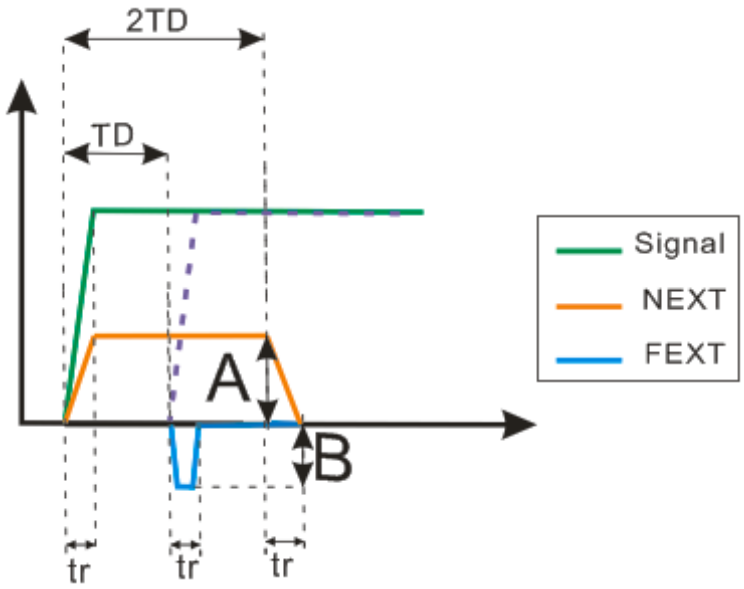


Fig.2.3.1 The equivalent circuit of crosstalk.

Fig.2.3.1 is the equivalent circuit of crosstalk [1], C_m is mutual capacitance, L_m is mutual inductance and Z_o is characteristic impedance. $\overline{AB}$ is defined as Aggressor Line, and $\overline{CD}$ is defined as Victim Line. The crosstalk of Victim Line occurs nearby the source of Aggressor Line is called NEXT, and that occur close to the load side of Aggressor Line is called FEXT.



(a)



(b)

Fig2.3.2 (a) The scheme of crosstalk with terminated victim.

(b) NEXT caused by terminated victim.

The amplitude of the NEXT is determined by the Backward crosstalk coefficient (K_b) and the input voltage (V_{in}) of aggressor line. The pulse width of NEXT is two time longer than the propagation delay time of Victim Line. The amplitude value of FEXT is directly proportional to Forward crosstalk coefficient (K_f), the length of the parallel line (X), and input voltage of Aggressor Line, and inversely proportional to rise time of the input signal. [1][2]

Amplitude of NEXT:

$$A = \frac{V_{in}}{4}\left[\frac{Lm}{L} + \frac{Cm}{C}\right] \qquad (2.1)$$

Amplitude of FEXT:

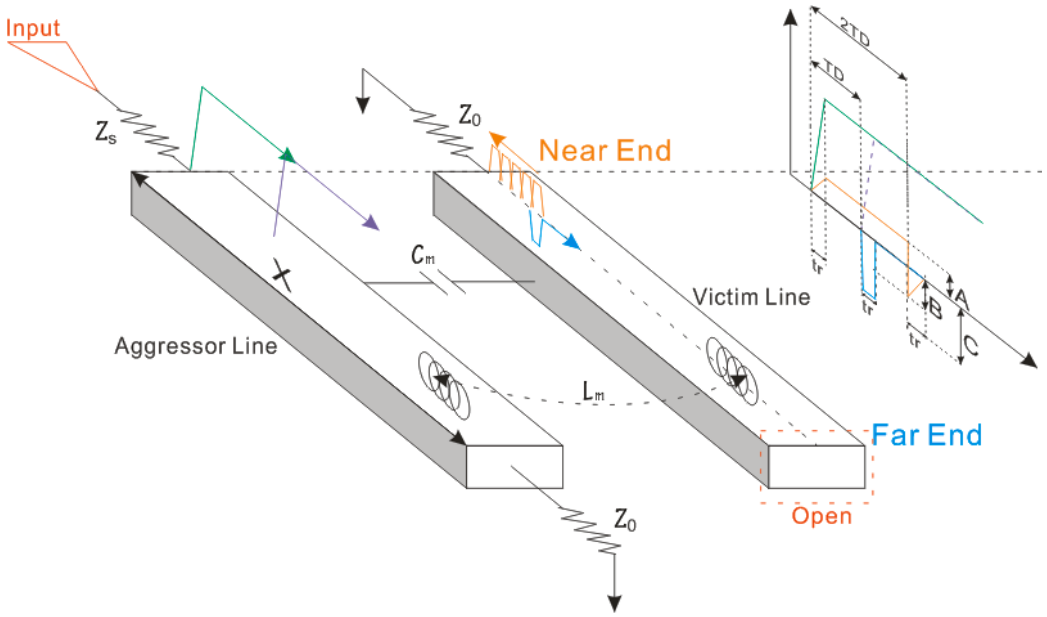
$$B = -\frac{V_{in} X \sqrt{LC}}{2tr}\left[\frac{Lm}{L} - \frac{Cm}{C}\right] \qquad (2.2)$$

Backward crosstalk coefficient:

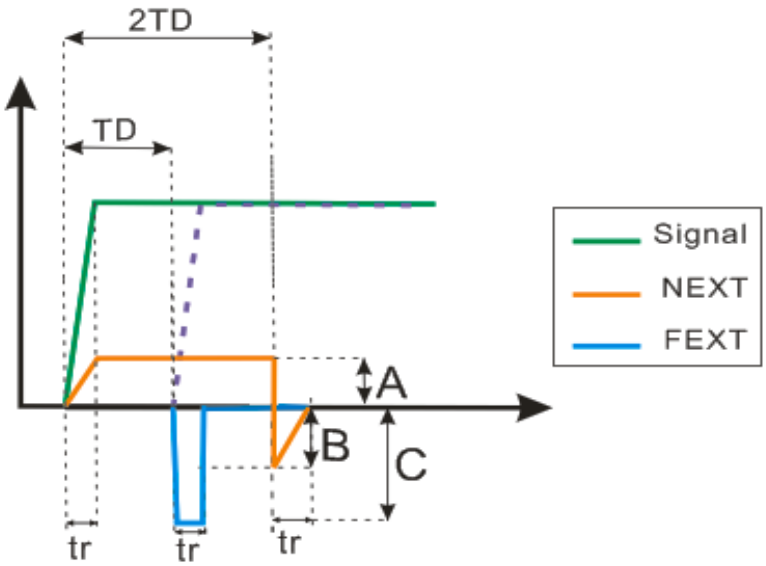
$$K_b = \frac{1}{4}\left(\frac{C_m}{C} + \frac{L_m}{L}\right) \qquad (2.3)$$

Forward crosstalk coefficient:

$$K_f = -\frac{\sqrt{LC}}{2}\left(\frac{L_m}{L} - \frac{C_m}{C}\right) \qquad (2.4)$$



(a)



(b)

Fig2.3.3 (a) The scheme of crosstalk with open victim.

(b) NEXT caused by open victim.

Amplitude of NEXT:

$$A = \frac{V_{in}}{4}\left[\frac{Lm}{L} + \frac{Cm}{C}\right] \quad (2.5)$$

$$B = \frac{1}{2}C \quad (2.6)$$

Amplitude of FEXT:

$$C = -\frac{V_{in}X\sqrt{LC}}{tr}\left[\frac{Lm}{L} - \frac{Cm}{C}\right] \quad (2.7)$$

Backward crosstalk coefficient:

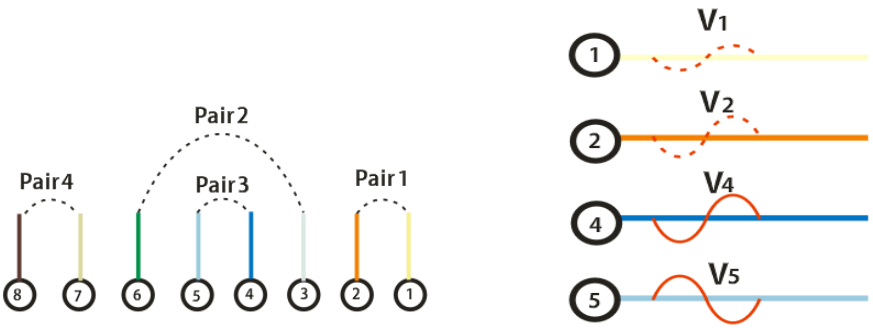
$$K_b = \frac{1}{4}\left(\frac{C_m}{C} + \frac{L_m}{L}\right) \quad (2.8)$$

Forward crosstalk coefficient:

$$K_f = -\frac{\sqrt{LC}}{2}\left(\frac{L_m}{L} - \frac{C_m}{C}\right) \quad (2.9)$$

2.4 Balancing the Crosstalk Noise

The twisted pair (UTP) structures are used for the CAT-6 cable system. The twisted structure of the cable provides the differential signal with balancing for reducing the capacitive crosstalk. The mutual capacitance is related to the structure of the joining point of two conductors and permittivity and loss of dielectric, cross-sectional structure, distance, length, and thickness of the lines. One of the methods of balancing the mutual capacitance is to insert the substantive capacitor between the lines embedded on PCB in modular jack. In this section, we will study on the method to balance the crosstalk noise.



(a) (b)

Fig.2.4.1 (a) Four pair of the UTP. (b) The capacitive coupling noise caused by wire 4, 5.

Fig.2.4.1 shows the four pair of the cable system. Wire 1 and 2, wire 3 and 6, wire 4 and 5, and wire 7 and 8 are the differential signal pair in the middle of the plug. Here, we focus on the two pair (1, 2), (4, 5). [3] [4] Wires1 and 2 construct a differential signal in the plug, and wires 4 and 5 pair construct another differential

signal pair. If a digital signal is transmitting on wires (1, 2) in the differential mode, the capacitive coupling noise occur in another wires (4, 5). A capacitive coupling noise voltage,V1, occurs on wire 1 and another capacitive coupling noise voltage,V2, occurs on wire 2, because of the differential signal voltage(V4, V5) on the differential signal pair (4, 5). The mutual capacitance between wire 2 and wire 4 is much greater than the mutual capacitance between wire 2 and wire 5, the capacitive coupling noise V2 has the same polarity as that of V4. For the same reason the capacitive coupling noise V1 has the same polarity as that of V4. The V1 does not equal V2 because of the difference of distance between the differential pair (4, 5) and wire 1 or 2, consequently the unbalanced mutual capacitance in wire 1 and 2 is generated. In a similar way, unbalanced capacitive crosstalk noise is generated in the other differential pair.

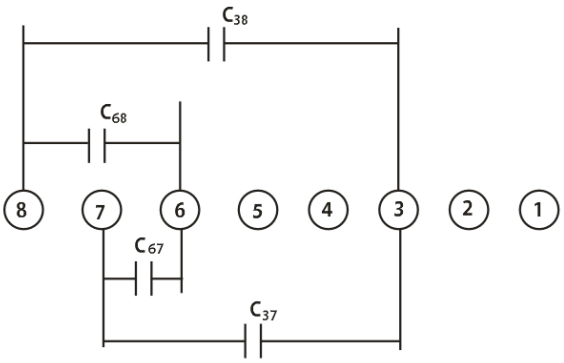


Fig.2.4.2

Fig.2.4.2. shows the mechanism of the unbalanced capacitive coupling noise that

cause by wiring arrangement in the untwisted region in the plug and in the insert. The mutual capacitance C67 is greater than the mutual capacitance C37. C68 is much greater than C38, and the mutual capacitances C37 and C38 were neglected. The balancing capacitance is necessary compensated between wires 6 and 8 with the value Cb = C67 - C68.

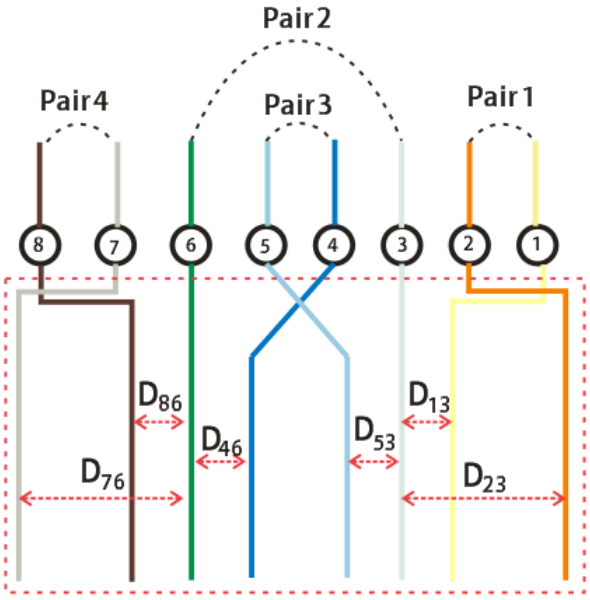


Fig.2.4.3

Fig.2.4.3 The method to compensate the capacitance generated in the plug is to change the distance of the unbalanced pairs. To move wire8 and wire4 close wire6, and wire5 and wire1 close wire3. The balancing capacitors, (Cb1= C23- C13); (Cb2 = C34 – C35); (Cb3 = C65 – C64); (Cb4 = C67 – C68), are generated by the change of distance.

CHAPTER 3

THE DESIGN OF THE CAPACITOR AND TRANSMISSION LINE ON PCB

3.1 Introduction

In order to compensate the unbalanced coupling capacitance, the balancing capacitors are added between each pair of transmission line on the PCB. The balanced capacitance of each wire results in the cancel of the crosstalk. The calculation of the coupling capacitance and the balancing must be accurate. However, it is difficult to control the balance because of the components of the modular jack exit other parasitic effect at 250MHz for category 6 specification. In addition to the parasitic effect, the layout of signal line on PCB is varied to fallow a variety of modular jack, and it is hard and complicated to calculate and adjust. In this chapter, we design the capacitors to compensate on PCB and employ the EDA tool “ADS 2006a” and “Momentum” to extract the characteristic of the balanced capacitor. Consequently, we verify with the complete product of the capacitor. The design procedure is as follows.

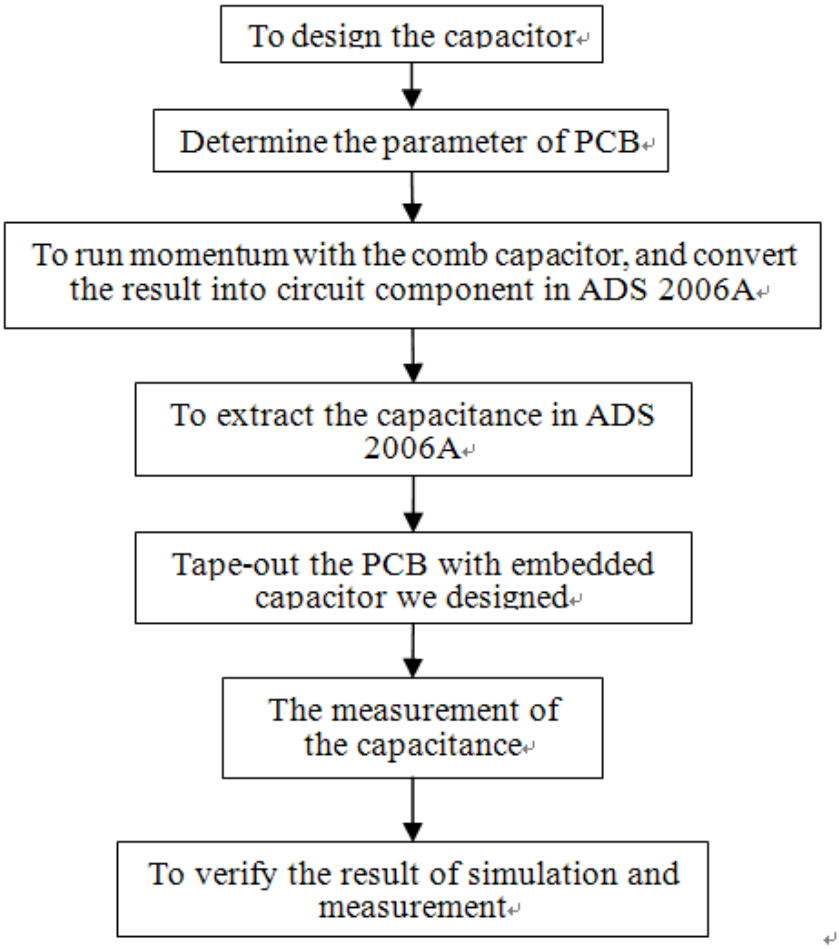
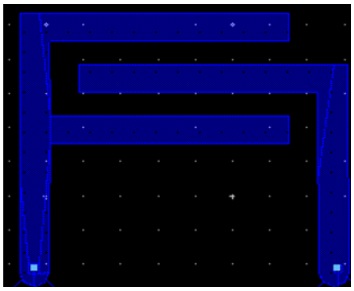


Fig.3.1.1 The design procedure of capacitor

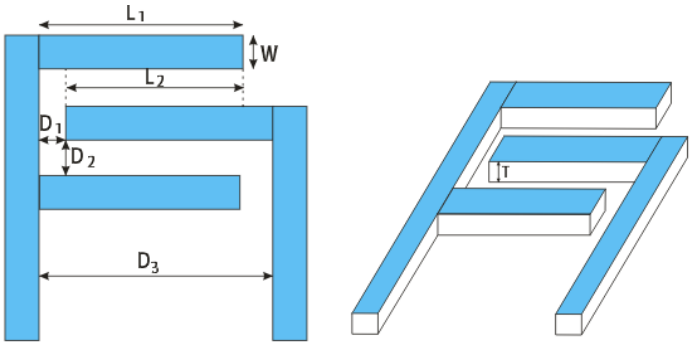
3.2 Design of Capacitors

For the effective capacitance on the double layer PCB a comb structure is utilized, because of the structure of parallel-plate on the thick PCB is not suitable to generate the appropriate capacitance. Initially, design the basic comb capacitor and then set the variable for designing. We change one variable and fix the others for eight cases to design.



N	L1	L2	W	D1	D2	D3	T
3	64 mil	56 mil	8 mil	7 mil	8 mil	72 mil	1.4 mil

(a)



(b)

Fig.3.2.1 (a) Layout of the basic unit. (b) Variable of the basic unit.

W: Width of the line.

L1: Length of the teeth.

L2: Interleaving length.

D1: Distance between teeth and line.

D2: Distance between two teeth.

T: Thickness.

N: Number of the teeth.

The scheme of the PCB we used to imbed the comb capacitor and signal wire is shown in Fig.3.2.2.

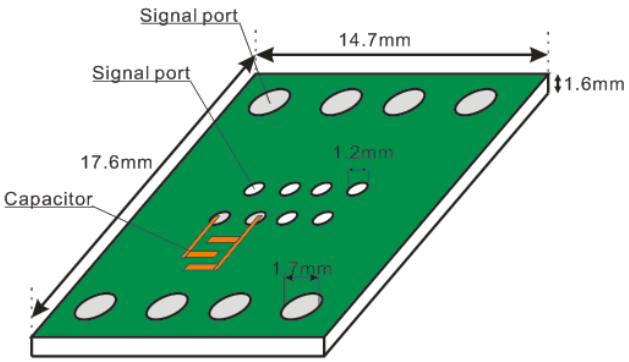
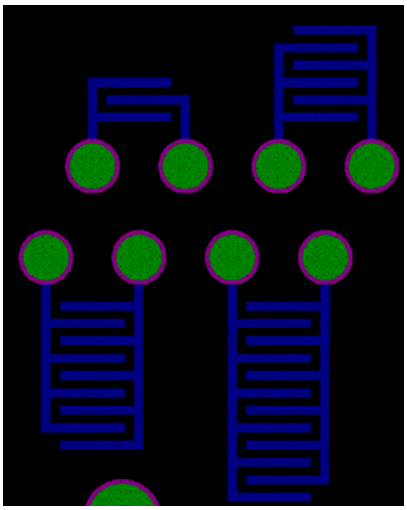


Fig.3.2.2

Fig.3.2.3~Fig.3.2.10 show the CASE.1~CASE.8. In the CASE.1, we change the number of tooth and fix other variables to observe the influence of the teeth number for capacitance. Similarly, In CASE.2 the line width is changed, the distance between the teeth is changed in CASE.3, the length of the teeth is changed in CASE.4, and the distance between teeth and line and fixed the interleaving length is changed in CASE.5. The distance between the capacitor and the signal port is considered in CASE.6. Furthermore, the capacitors located on top and bottom layer is overlapping entirely in CASE.7, and the capacitors of top layer and bottom layer are cross overlapping in CASE.8.

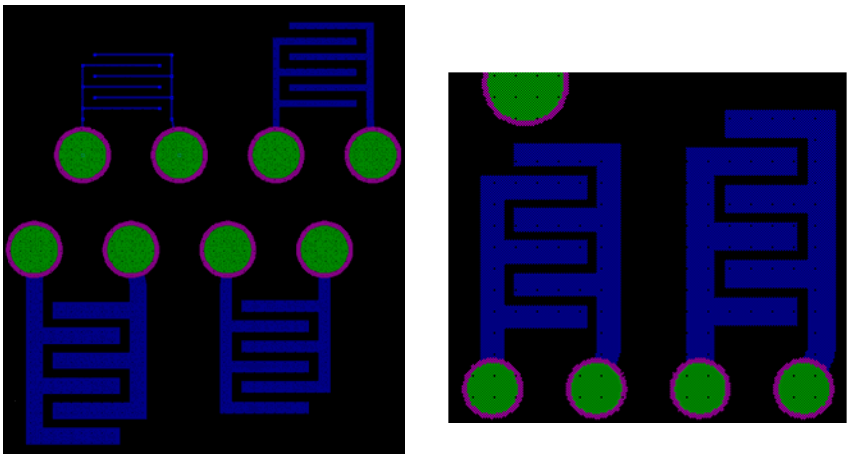
CASE.1



N	L1	L2	W	D1	D2	D3	T
3, 6, 9, 12, 15	64 mil	56 mil	8 mil	8 mil	7 mil	72 mil	1.4 mil

Fig.3.2.3

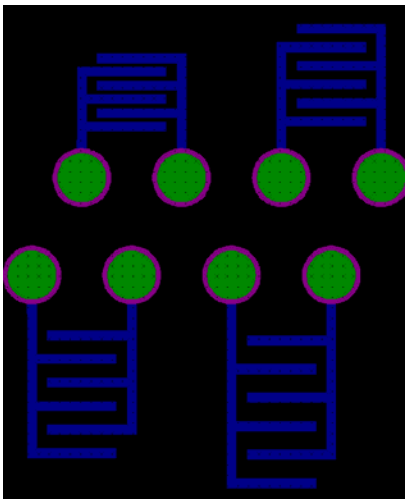
CASE.2



N	L1	L2	W	D1	D2	D3	T
6	64 mil	56 mil	2, 6, 10, 14, 18, 22mil	8 mil	7 mil	72 mil	1.4 mil

Fig.3.2.4

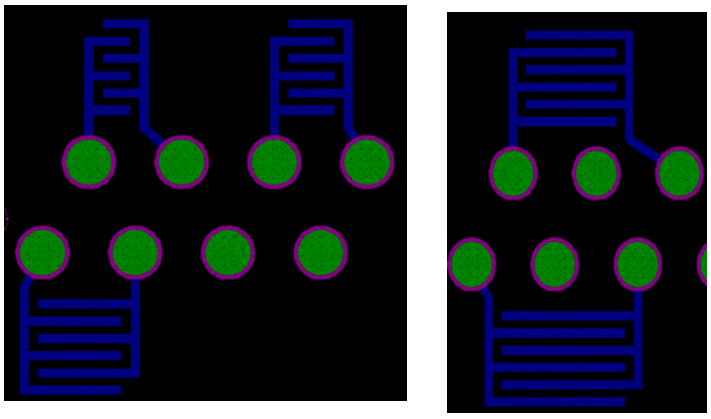
CASE.3



N	L1	L2	W	D1	D2	D3	T
6	64 mil	56 mil	8 mil	8 mil	3, 7, 11, 15 mil	72 mil	1.4 mil

Fig.3.2.5

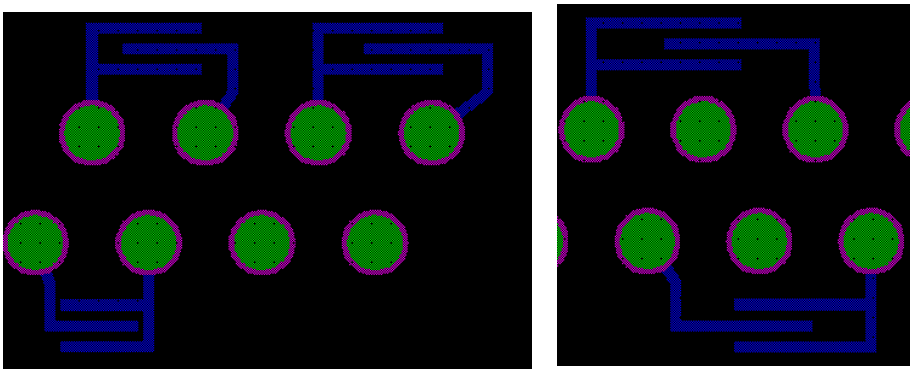
CASE.4



N	L1	L2	W	D1	D2	D3	T
6	32, 48, 80, 96, 128, 192 mil	24, 40, 72, 88, 120, 184 mil	8 mil	8mil	7 mil	40, 56, 88, 104, 136, 200 mil	1.4 mil

Fig.3.2.6

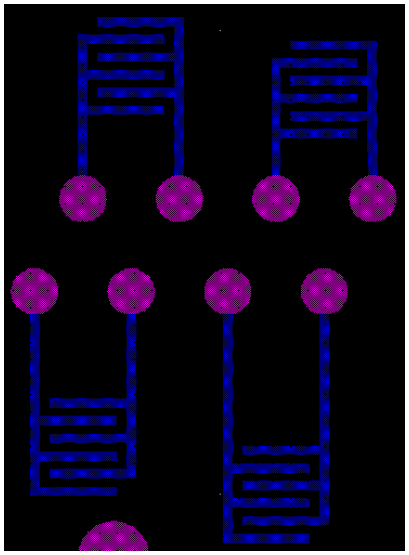
CASE.5



N	L1	L2	W	D1	D2	D3	T
6	59, 74, 84, 94, 104 mil	56 mil	8 mil	3,18,28,38,48 mil	7 mil	62, 92, 112, 132, 152 mil	1.4 mil

Fig.3.2.7

CASE.6

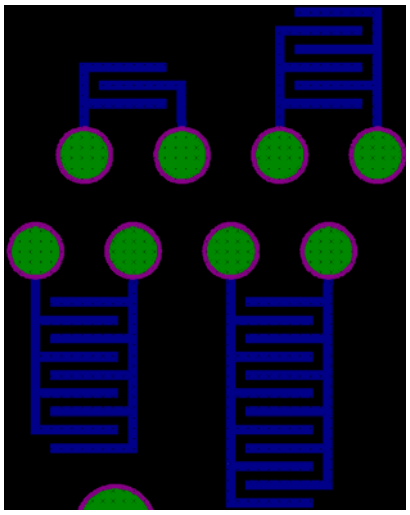


N	L1	L2	W	D1	D2	D3	T	D4
6	64 mil	56 mil	8 mil	8 mil	7 mil	72 mil	1.4 mil	40, 60, 80 ,120 mil

D4: distance between capacitor and port.

Fig.3.2.8

CASE7

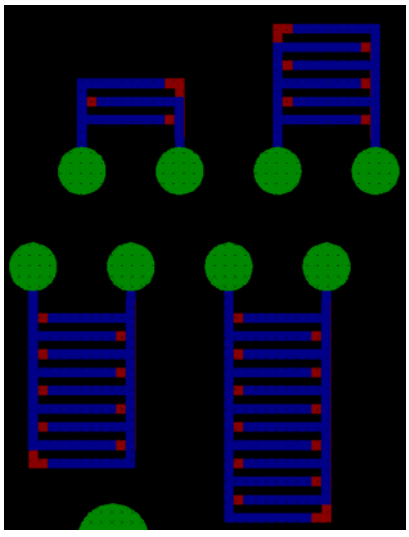


N	L1	L2	W	D1	D2	D3	T
6,	64 mil	56 mil	8 mil	8 mil	7 mil	72 mil	1.4 mil

Top and bottom layer are overlapping

Fig.3.2.9

CASE.8



N	L1	L2	W	D1	D2	D3	T
6,	64 mil	56 mil	8 mil	8 mil	7 mil	72 mil	1.4 mil

Top and bottom layer are cross overlapping

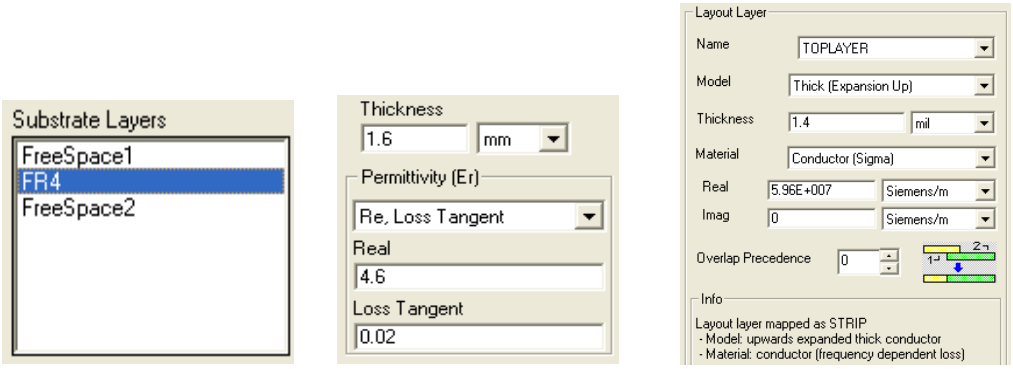
Fig.3.2.10

3.3 Simulation of Capacitors

We use “Advance Design System 2006A” for pre-calculating the capacitance, and initially, to deal with the capacitor we designed by “Momentum”. “Momentum” is planar electro-magnetic analytic soft which is a part of “ADS2006A”. It can analyze the layout with any shape of multi-layer structure by layout-driven mod and generates the exact EM model after the magnetic simulation with S-parameter result, which put the coupling and parasitic effect into consideration automatically. The result will be used for the application of circuit analysis and show the distribution of surface current and Far Field Range. The material of PCB is FR4 and simulated using the parameter given in Table I, the setting of substrate is shown in Fig.3.3.1

TABLE I

Parameter of PCB	
Thickness	1.6 mm
Permittivity	4.6
Loss Tangent	0.02
Permeability	1
Thickness of copper	1.4 mil
Conductivity of copper	5.96E+007 Siemens/m



(a) (b)

Fig.3.3.1 (a) The substrate and the parameter of FR4. (b) The parameter of top layer which material is copper.

.

The process of momentum is as fallow steps

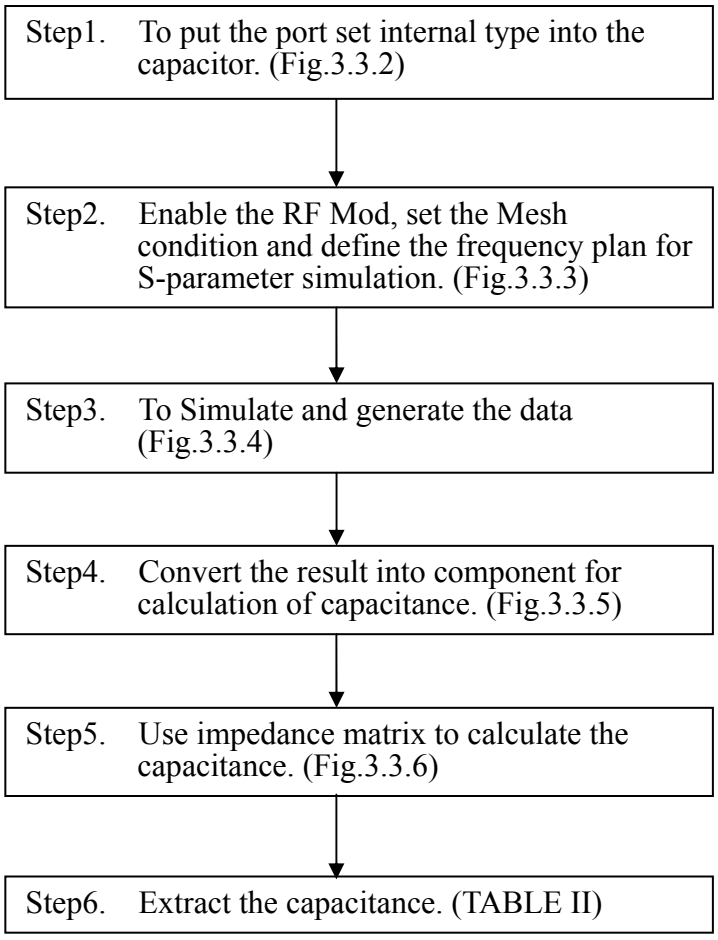


Fig.3.3.2. The process of momentum.

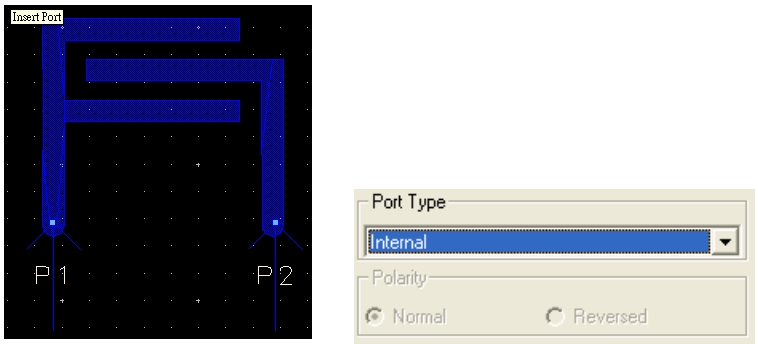
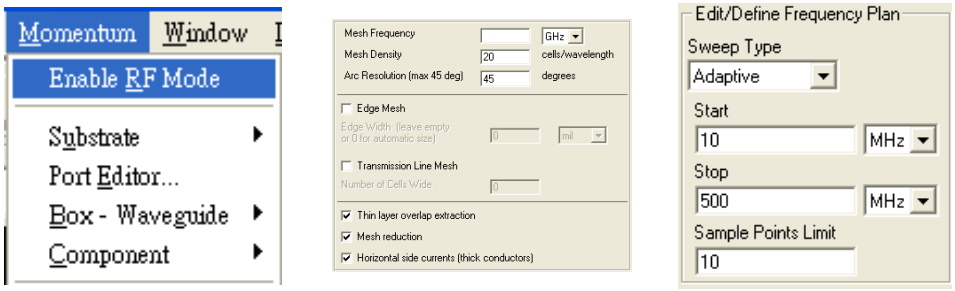


Fig.3.3.3 Insert the port set internal type into the capacitor.



(a) (b) (c)

Fig.3.3.4 (a) Enable RF mode. (b) Mesh setting (c) Edit frequency plan

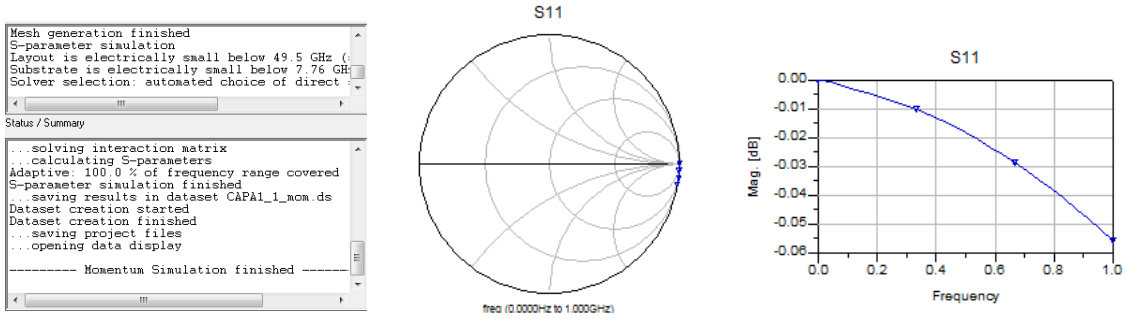


Fig.3.3.5 The simulation and result with s-parameter and smith chart

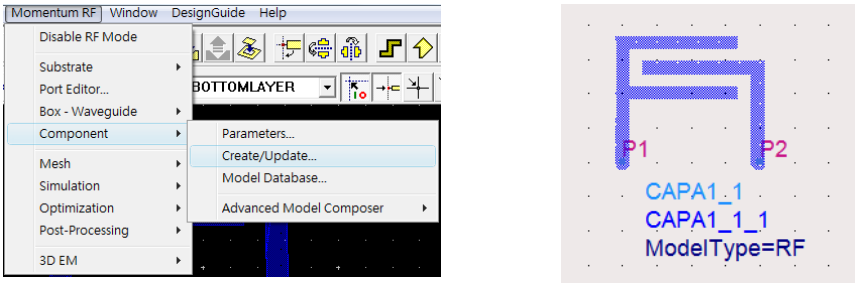


Fig.3.3.6 Convert the characteristic of capacitor into component.

We transform the scattering matrix result from momentum to an impedance matrix for extraction of the capacitance. The syntax is as fallow.

Define the impedance matrix

$$Z_t = \text{stoz}(S)$$

Set the input impedance Z_{in}

$$Z_{in} = \frac{[Z_t(1,1) - Z_t(2,1)Z_t(1,2)]}{Z_t(2,2)}$$

C_{in} is the capacitance

$$C_{in} = \frac{-1}{2\pi \times \text{freq} \times \text{imag}(Z\_in)}$$

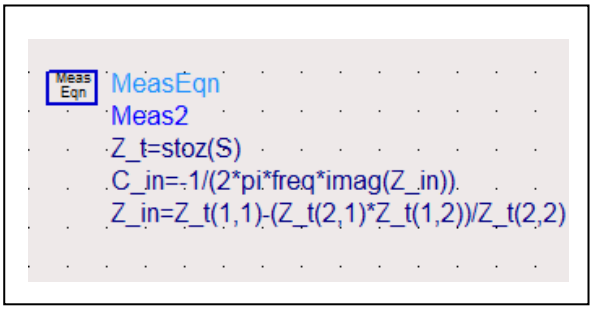


Fig.3.3.7 The syntax to extract capacitance.

The simulated result of capacitance is as fallow

TABLE II

CASE.1					
N	3	6	9	12	15
C_{in}	0.22 pF	0.35 pF	0.51 pF	0.63 pF	0.8 pF

CASE.2					
W	6 mil	10 mil	14 mil	18 mil	22 mil
C_{in}	0.31 pF	0.38 pF	0.42 pF	0.46 pF	0.51 pF

CASE.3				
D2	3 mil	7 mil	11 mil	15 mil
C_{in}	0.39 pF	0.35 pF	0.33 pF	0.33 pF

CASE.4					
L1	32 mil	48 mil	80 mil	96 mil	128 mil
C_{in}	0.22 pF	0.28 pF	0.4 pF	0.45 pF	0.59 pF

CASE.5					
D1	8 mil	18 mil	28 mil	38 mil	48 mil
C_{in}	0.22 pF	0.22 pF	0.22 pF	0.23 pF	0.22 pF

CASE.6					
D4	27 mil	40 mil	80 mil	60 mil	120 mil
C_{in}	0.35 pF	0.35 pF	0.36 pF	037 pF	0.4 pF

CASE.7				
N	3	6	9	12
C_{in}	0.4 pF	0.63 pF	0.93 pF	1.2 pF

CASE.8				
N	3	6	9	12
C_{in}	0.4 pF	0.65 pF	0.93 pF	1.2 pF

3.4 Measurement Data and Simulation Result

These capacitors were implemented after the design of ADS. We contrast the measurement data with simulation result and analyze whether the trend be consistent or not. Therefore, we should combine the simulation and practice for prospective performance. An aerial view of the capacitors embedded on PCB is shown in Fig.3.4.1. Due to the limit of the PCB structure, we must design the cal kit and fixture for the PCB.

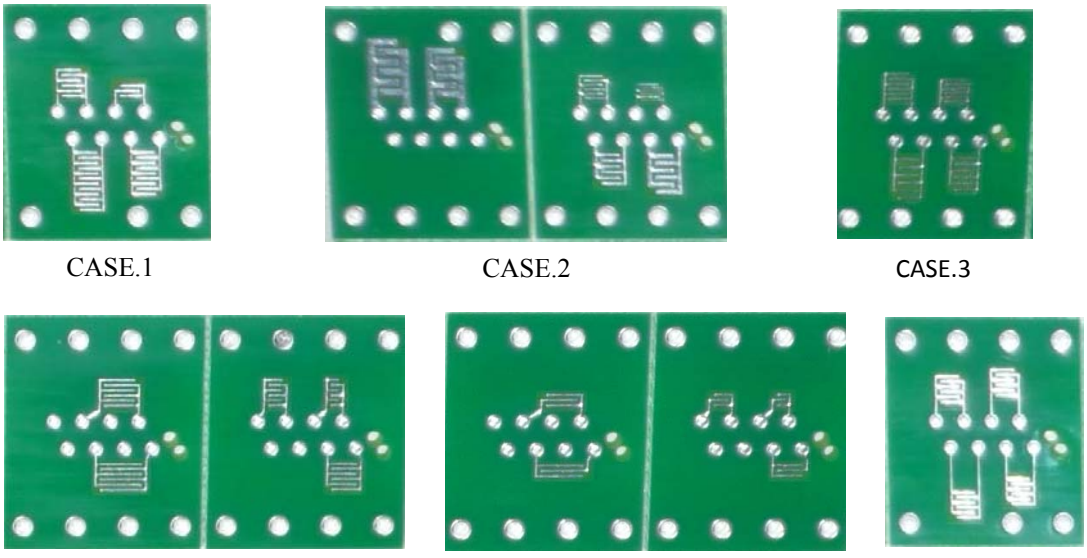


Fig.3.4.1 The finished capacitor on PCB, here shows CASE.1~6

The cal kit for the PCB is shown to Fig.3.4.2

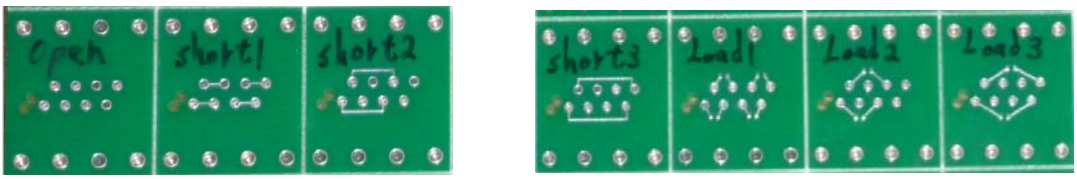
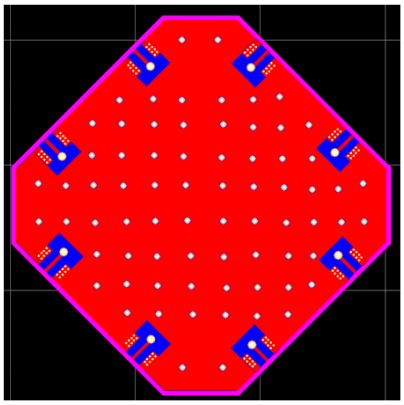
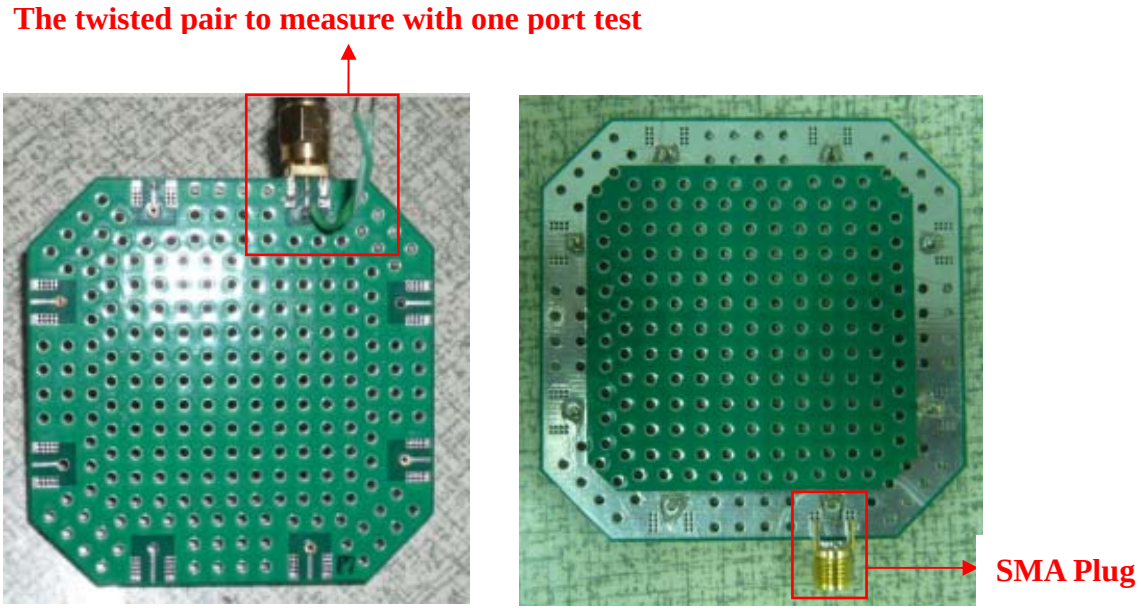


Fig.3.4.2 The cal kit.

The fixture for measurement is referred to Fig.3.4.3



(a)



(b)

Fig.3.4.3 (a) Shows the layout of fixture we design.

(b) A fixture is combined with SMA Plug and UTP.

The measurement work is finished by Agilent N5230A PNA-L Network Analyzer shown in fig.3.4.4. The complete view of the measurement is shown in Fig.3.4.5 TABLE III briefly describes the setting of PNA-L Network Analyzer.

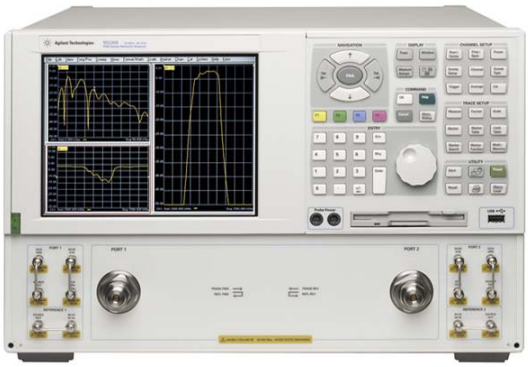


Fig.3.4.4 Agilent N5230A PNA-L Network Analyzer.

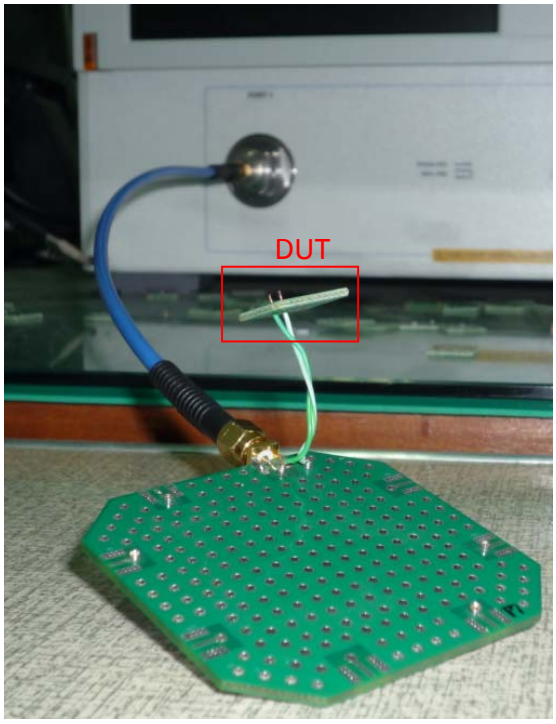
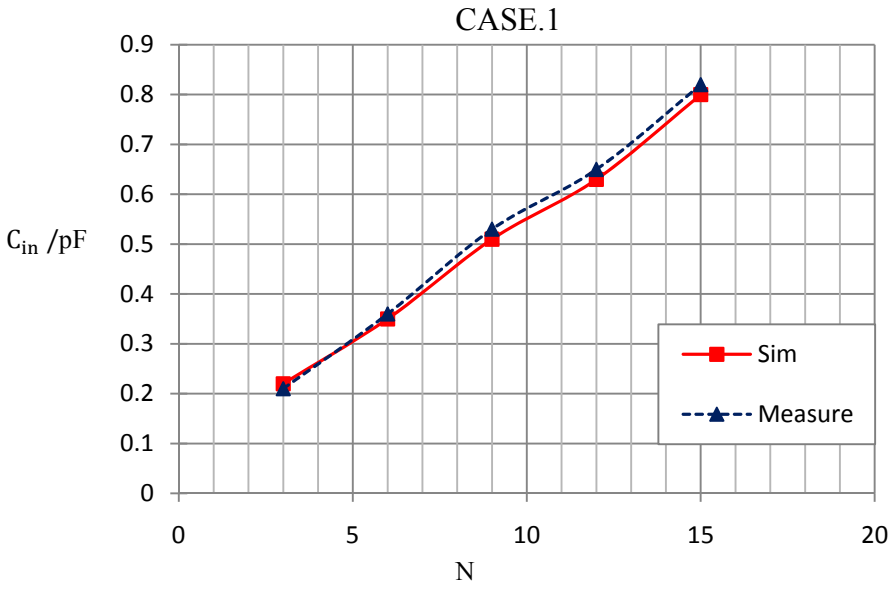


Fig.3.4.5 Complete view of the measurement system.

Table III

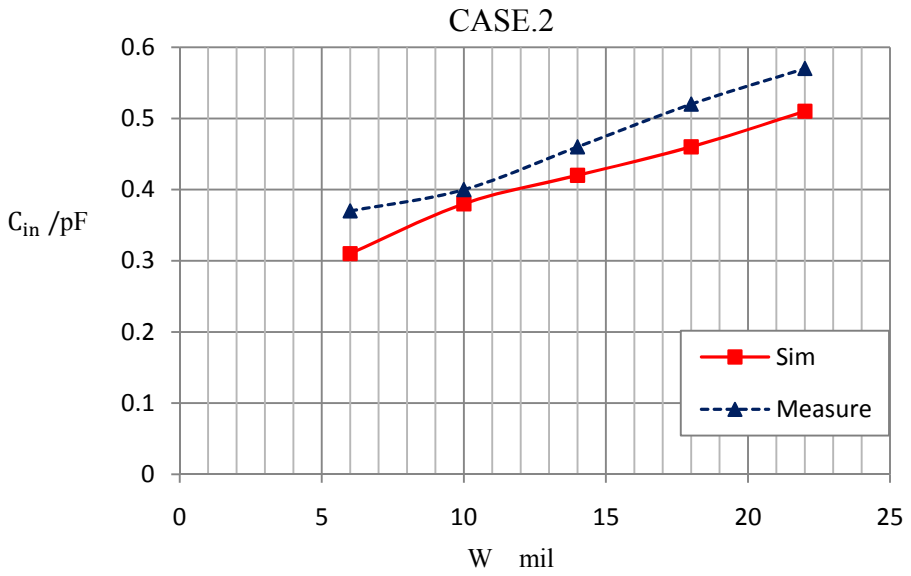
Parameters	Values
Frequency range	10MHz~500MHz
Power	0 dB
Impedance	50 ohm
Sample Point	401
Band Width	300

The measurement has error capacitance from the UTP about 0.55 pF at 250MHz after calibration. We deduct the error from the data at 250MHz and capture the value adjusted to contrast with the simulated value of capacitance at 250MHz. The capacitance from measurement and simulation at 250MHz is shown as fallow.



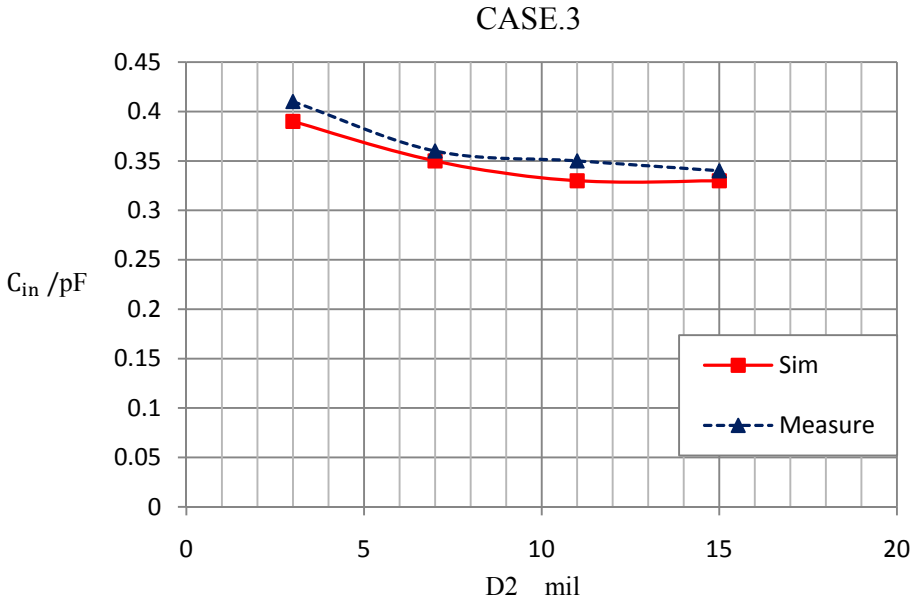
CASE.1					
N	3	6	9	12	15
Simulation	0.22 pF	0.35 pF	0.51 pF	0.63 pF	0.8 pF
Measurement	0.21 pF	0.36 pF	0.53 pF	0.65 pF	0.82 pF

Fig.3.4.6 Measurement data and simulation results of CASE.1 at 250MHz



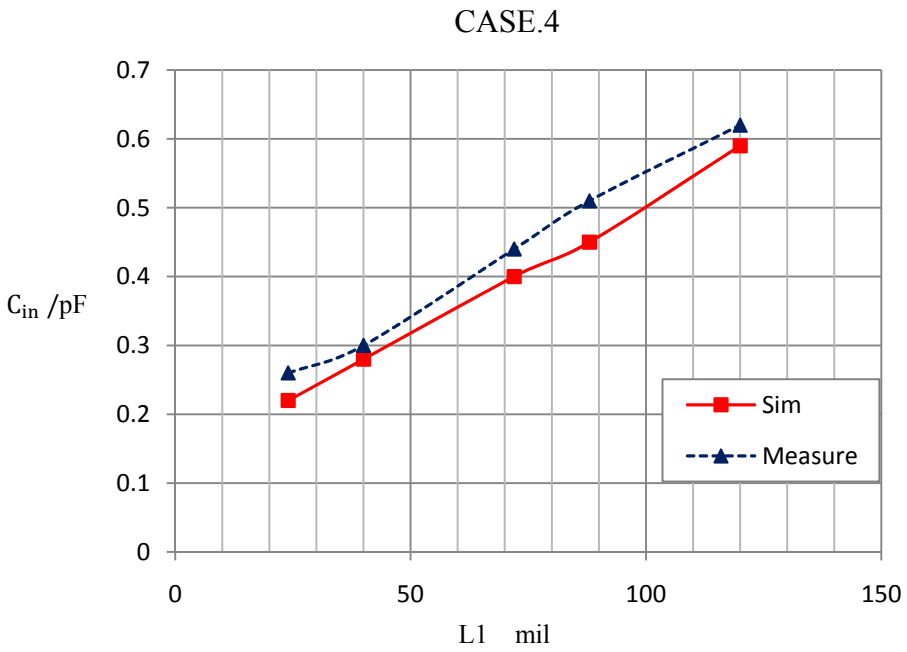
CASE.2					
W	6 mil	10 mil	14 mil	18 mil	22 mil
Simulation	0.31 pF	0.38 pF	0.42 pF	0.46 pF	0.51 pF
Measurement	0.37 pF	0.4 pF	0.46 pF	0.52 pF	0.57 pF

Fig.3.4.7 Measurement data and simulation results of CASE.2 at 250MHz



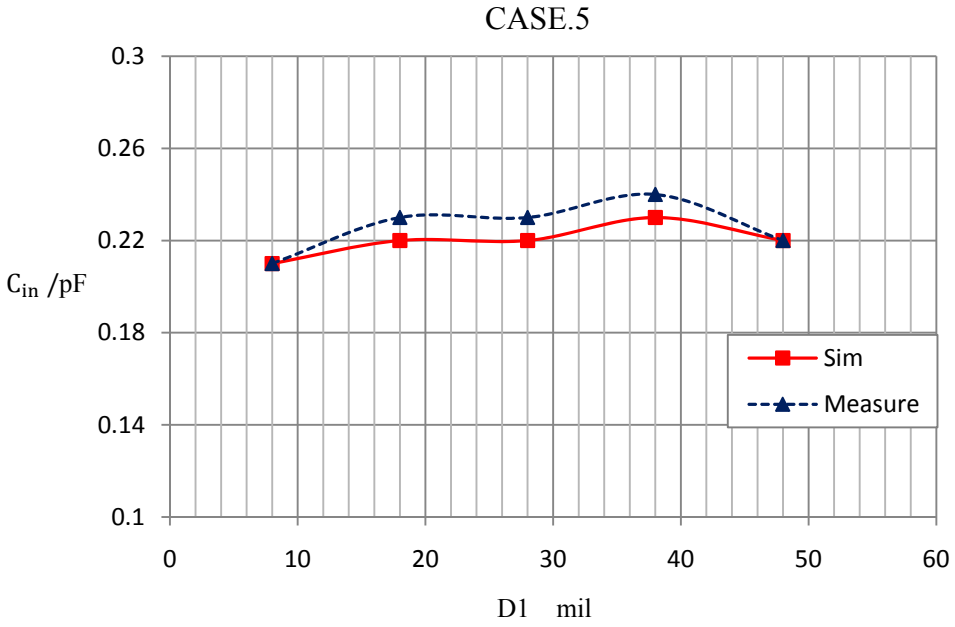
CASE.3				
D2	3 mil	7 mil	11 mil	15 mil
Simulation	0.39 pF	0.35 pF	0.33 pF	0.33 pF
Measurement	0.41 pF	0.36 pF	0.35 pF	0.34 pF

Fig.3.4.8 Measurement data and simulation results of CASE.3 at 250MHz



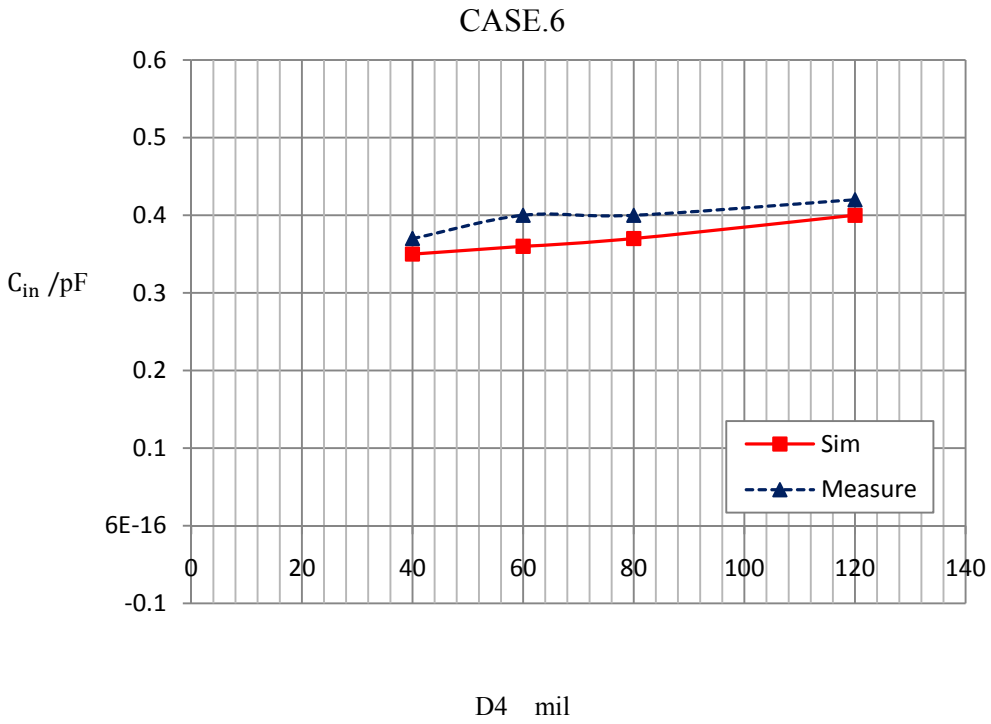
CASE.4					
L1	24 mil	40 mil	72 mil	88 mil	120 mil
Simulation	0.22 pF	0.28 pF	0.4 pF	0.45 pF	0.59 pF
Measurement	0.26 pF	0.3 pF	0.44 pF	0.51 pF	0.62 pF

Fig.3.4.9 Measurement data and simulation results of CASE.4 at 250MHz



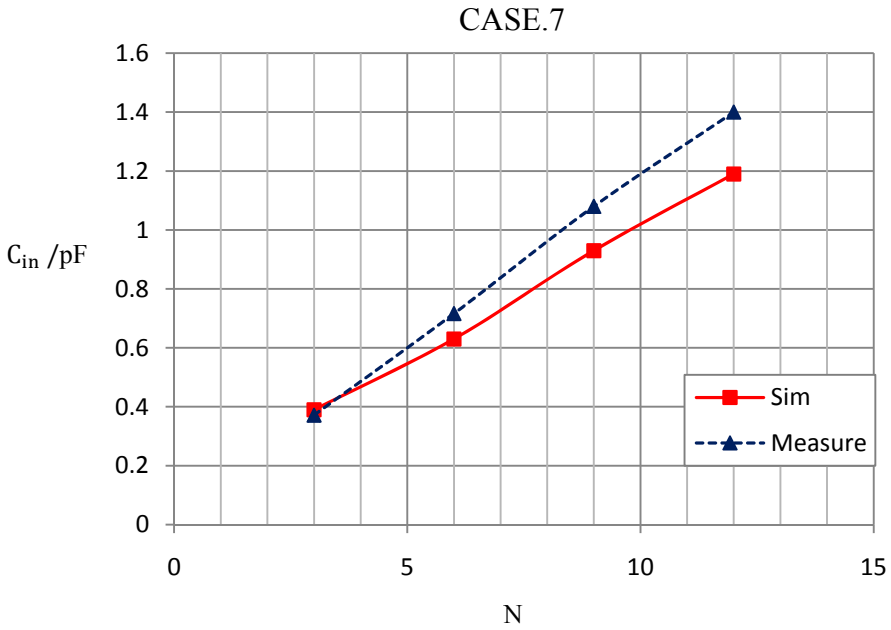
CASE.5					
D1	8 mil	18 mil	28 mil	38 mil	48 mil
Simulation	0.21 pF	0.22 pF	0.22 pF	0.23 pF	0.22 pF
Measurement	0.21 pF	0.23 pF	0.23 pF	0.24 pF	o.22 pF

Fig.3.4.10 Measurement data and simulation results of CASE.5 at 250MHz



CASE.6				
D4	40 mil	80 mil	60 mil	120 mil
Simulation	0.35 pF	0.36 pF	037 pF	0.4 pF
Measurement	0.37 pF	0.4 pF	0.4 pF	0.42 pF

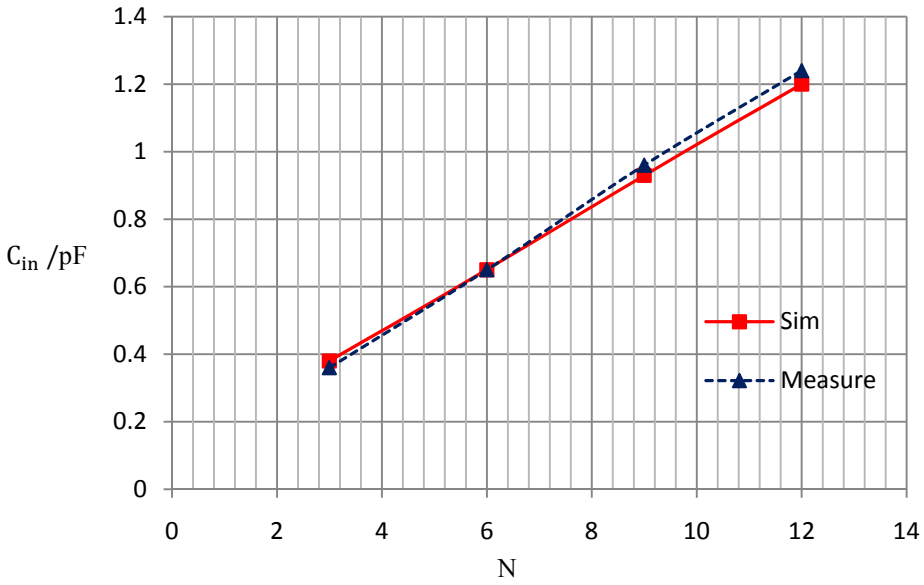
Fig.3.4.11 Measurement data and simulation results of CASE.6 at 250MHz



CASE.7				
N	3	6	9	12
Simulation	0.4 pF	0.63 pF	0.93 pF	1.2 pF
Measurement	0.37 pF	0.7 pF	1.08 pF	1.4 pF

Fig.3.4.12 Measurement data and simulation results of CASE.7 at 250MHz

CASE.8



CASE.8				
N	3	6	9	12
Simulation	0.4 pF	0.65 pF	0.93 pF	1.2 pF
Measurement	0.37 pF	0.7 pF	1.08 pF	1.4 pF

Fig.3.4.13 Measurement data and simulation results of CASE.8 at 250MHz

3.5 CONCLUSION

The purpose to designing the capacitors on PCB is to understand the characteristic of capacitor on PCB and build the simulation environment conform the true situation. At last, we find the capacitance we required for compensating to reduce the NEXT. We use balun to generate differential signal and measured by the Network analyzer. The layout of capacitors is designed by Protel99 and simulated in ADS2006. The results of simulation and measurement are similar and the simulation environment can be used for designing the capacitor exactly on PCB.

CHAPTER 4

THE SIMULATION RESULT AND MEASUREMENT DATA FOR THE TRANSMISSION LINE WITH COMPENSATION OF CAPACITANCE

4.1 Introduction

Recently, Modern network products have been developed to hold more bandwidth, more internet access, and higher speed. These purposes challenge designers to have effective method to support the trend of complexity in products. The compensation on PCB can reduce the crosstalk occurred in the untwisted region of RJ45 connector, however, the wire on PCB also generates capacitive coupling noise and other effects to interfere the calculation of the compensated capacitance. In addition to the effects on PCB, the component and geometry of RJ45 Jack increase the difficulty in designing. The old way of trial- and -error design practices is no longer acceptable today. It must be more effective to design the products from the first time through the design cycle. In this chapter, the tool ADS2006A is used to design the layout of wire on PCB with established framework and build the model of RJ45 jack for the effective design. The design flow is shown in Fig.4.1.1

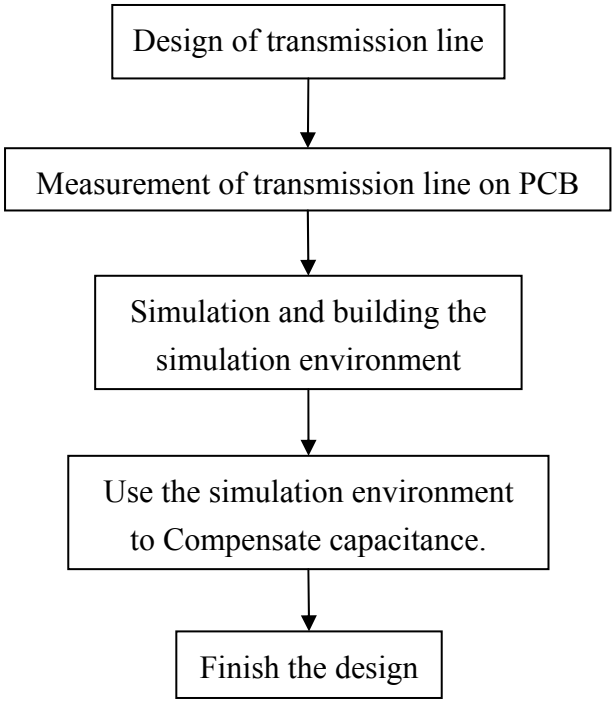


Fig.4.1.1

4.2 Design and Measurement of Transmission Line on PCB

The PCB in RJ45 jack is used for compensating, however, the density of the wire on PCB causes the problem of crosstalk and on-board parasitic capacity. Because of the limit of structure and fixed signal position on PCB, we only consider the path width of wire. Fig.4.2.1 shows the location of the signal port on PCB.

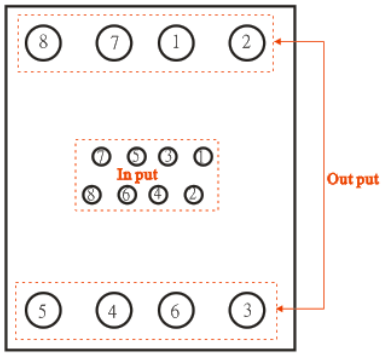


Fig4.2.1

We decrease the density of wire for less parasite capacity and scatter the wire for less crosstalk on PCB. Fig4.2.2 shows the layout of trace and the finished product. The width of the signal wire is 8mil, and we put the wire on the same layer for the convenience of compensation on another layer. [5][6]

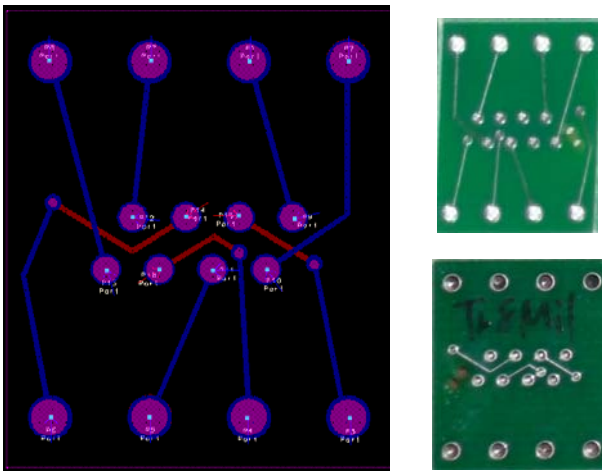


Fig.4.2.2

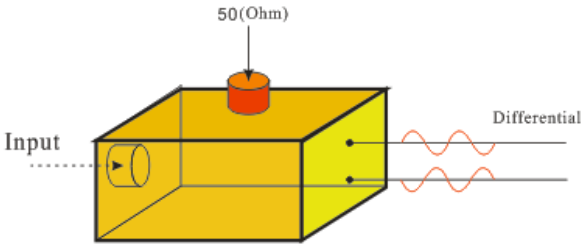
The measurement work is started after finishing the product. The measurement must utilize CAT-6 cabling meet all of the requirements of TIA/EIA-568-B.2-1 and its respective addenda [7]. The specification of Connecting hardware pair-to-pair NEXT loss for CAT-6 is determine using (4.1), where f [MHz] is the measurement frequency, and the value is shown in TABLE.IV.

$$\mathrm{NEXT}_{\mathrm{conn}} \geq 54 - 20\log\left(f/100\right)\mathrm{dB} \tag{4.1}$$

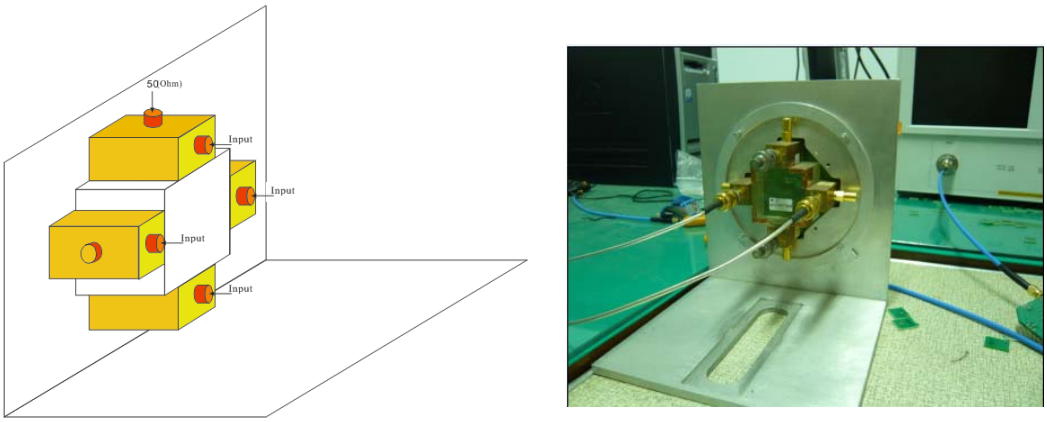
TABLE.IV

Frequency (MHz)	NEXT loss (dB)
1.0	75.0
4.0	75.0
8.0	75.0
10.0	74.0
16.0	69.9
20.0	68.0
25.0	66.0
31.25	64.1
62.5	58.1
100.0	54.0
200.0	48.0
250.0	46.0

The instrument for the measurement is Agilent PNA-L Network Analyzer, and two balun transformers are used for accurate transmission measurements of the balanced twisted pair cables and connectors. Baluns are arranged at orthogonal locations on the ground plane.



(a)



(b)

Fig.4.2.3

The scheme for measuring the NEXT between two pairs is shown in Fig.4.2.4

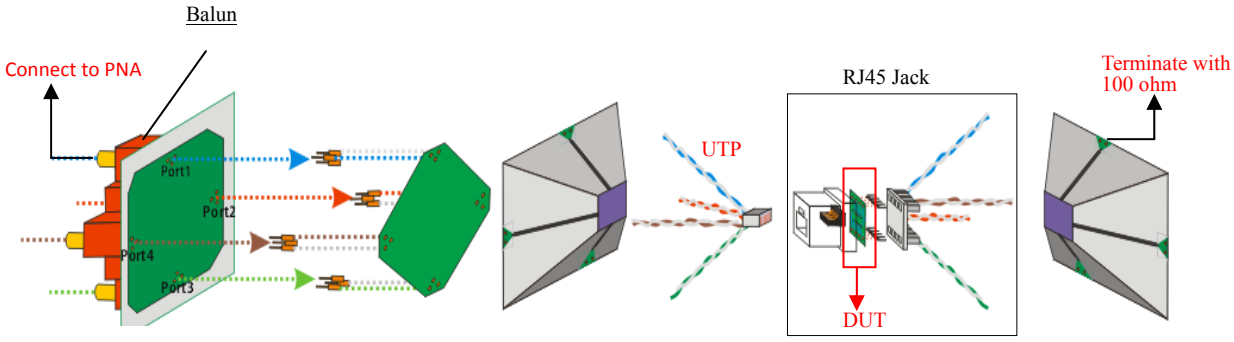
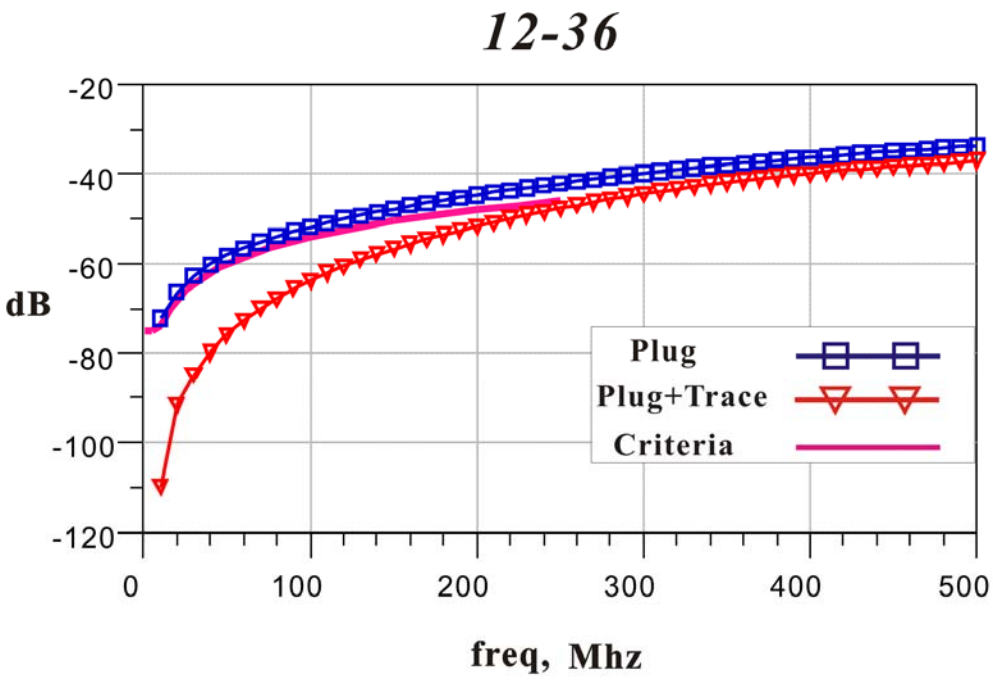


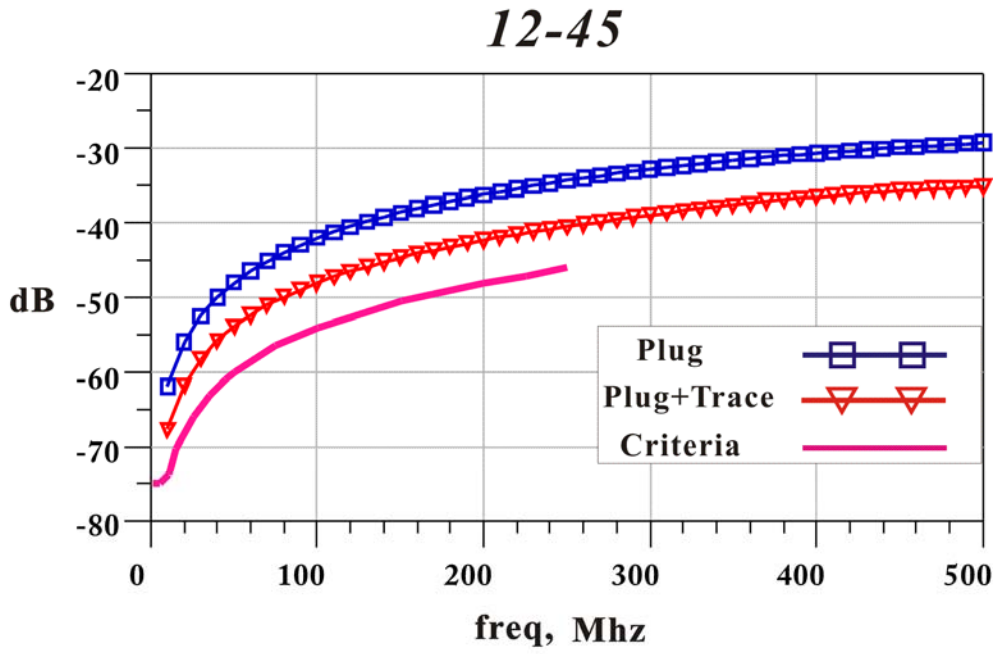
Fig.4.2.4.

The measurement system uses two input signal from PNA to balun which generate differential signal, and we use impedance 100ohm to terminate. The DUT is the PCB with wire we designed in RJ45 jack, and the data of connecting hardware pair-to-pair NEXT loss is measured. From the result, (12, 36), (36, 78), (45, 78) has been achieved the specificity of NEXT loss because of the method in ch3 being used for the insert.



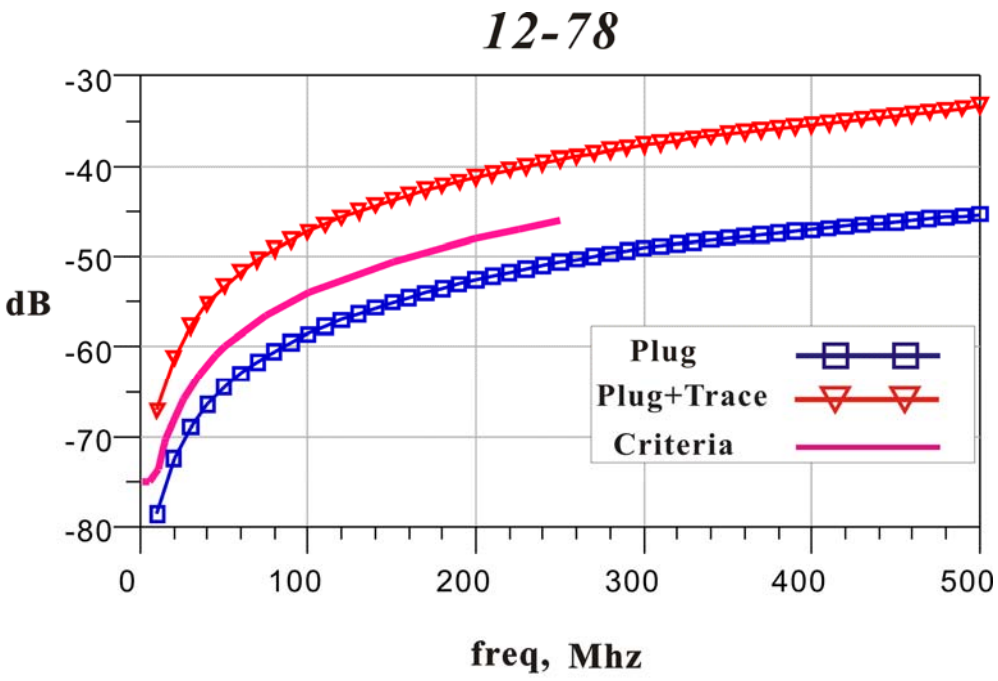
	Criteria	Plug	Plug+Trace
250 (Mhz)	-46 dB	-42.1 dB	-47.7 dB

Fig.4.2.5



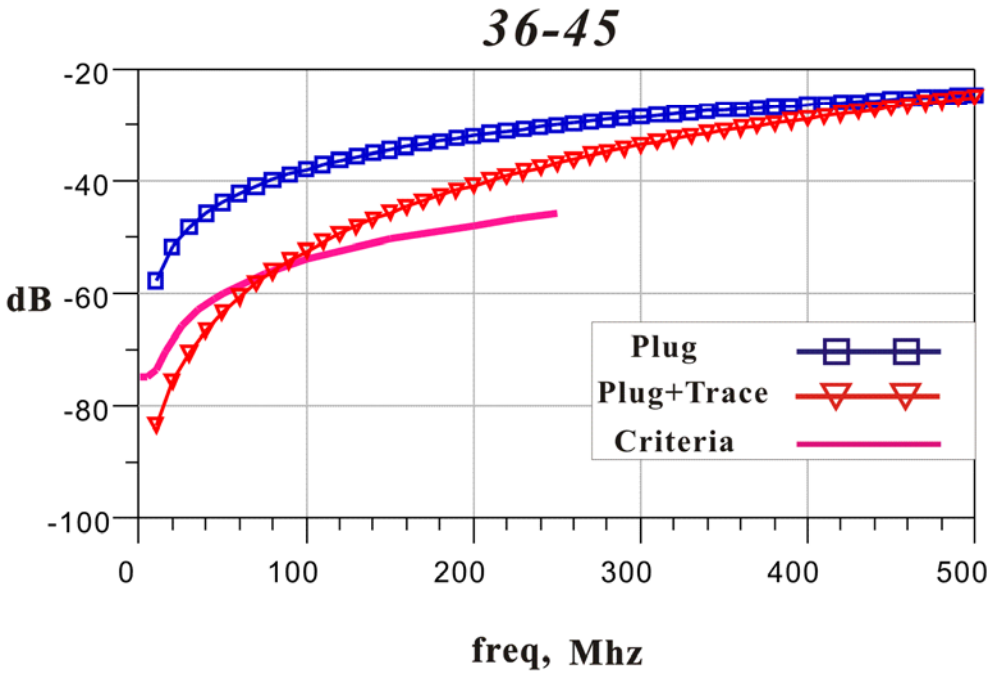
	Criteria	Plug	Plug+Trace
250 (Mhz)	-46 dB	-34.31dB	-40.4 dB

Fig.4.2.6



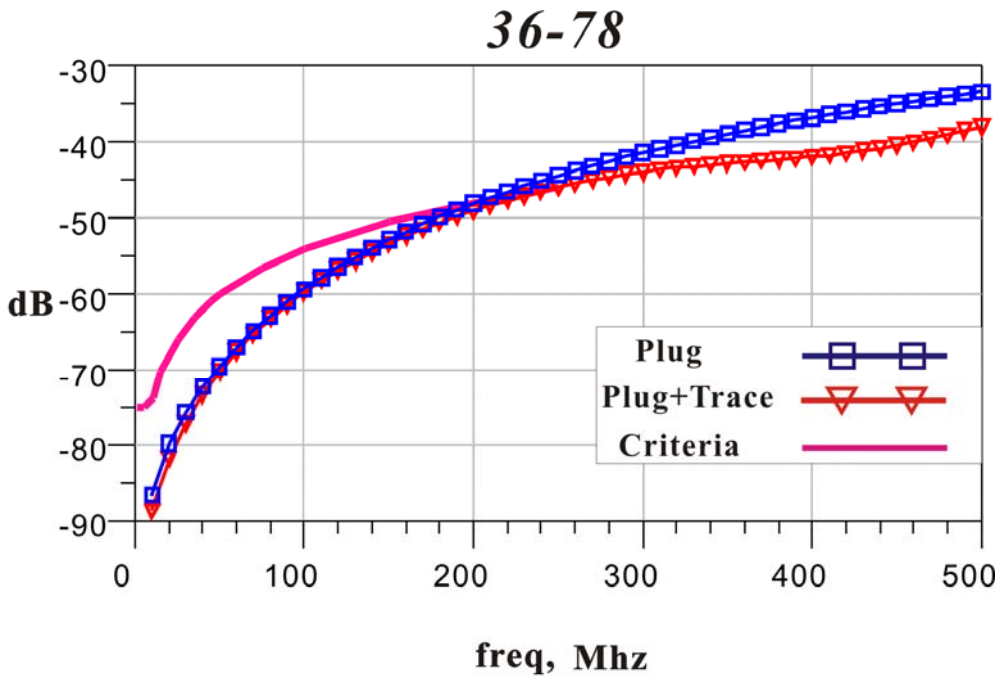
	Criteria	Plug	Plug+Trace
250 (Mhz)	-46 dB	-50.6 dB	-39.3 dB

Fig.4.2.7



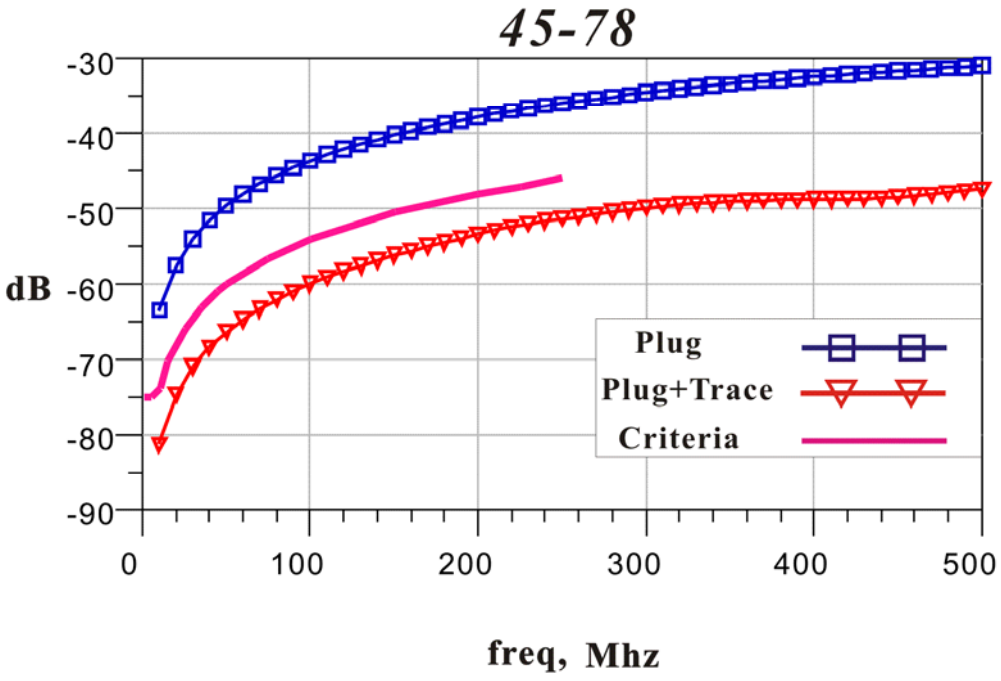
	Criteria	Plug	Plug+Trace
250 (Mhz)	-46 dB	-30.16 dB	-36.99 dB

Fig.4.2.8



	Criteria	Plug	Plug+Trace
250 (Mhz)	-46 dB	-44.37 dB	-45.9 dB

Fig.4.2.9



	Criteria	Plug	Plug+Trace
250 (Mhz)	-46 dB	-35.93 dB	-51.32 dB

Fig.4.2.10

4.3 Establishment of the Simulation Environment

The method for simulation has been shown in chapter 3. The electromagnetic behavior of transmission line on PCB will be extracted after the simulation by “Momentum”, and the result will be calculated. Fig.4.3.1 shows the setting of simulation used to calculate the NEXT loss. The setting is shown in TABLE.V. We use the circuit in Fig.4.3.1 to generate differential signal in the simulation environment and terminate the four pair with 100ohm, then run S-parameter to calculate the NEXT loss between every two pair on PCB. The result is shown in Fig.4.3.2. ~Fig.4.3.7.

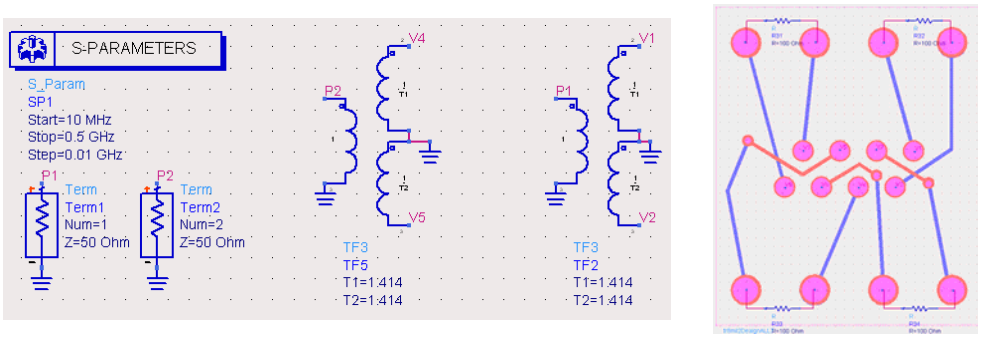
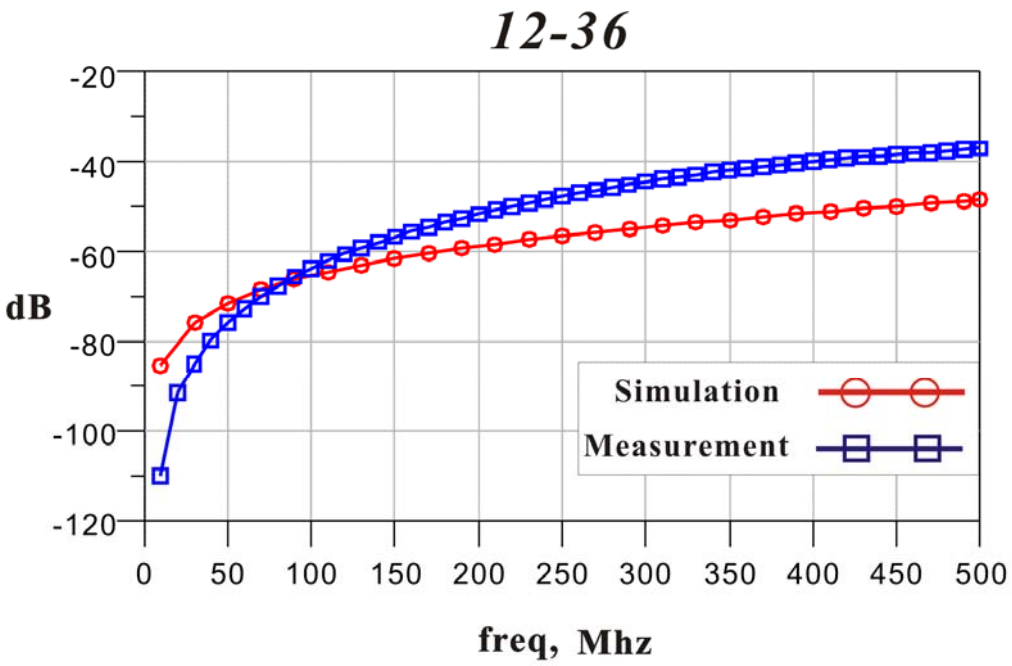


Fig.4.3.1

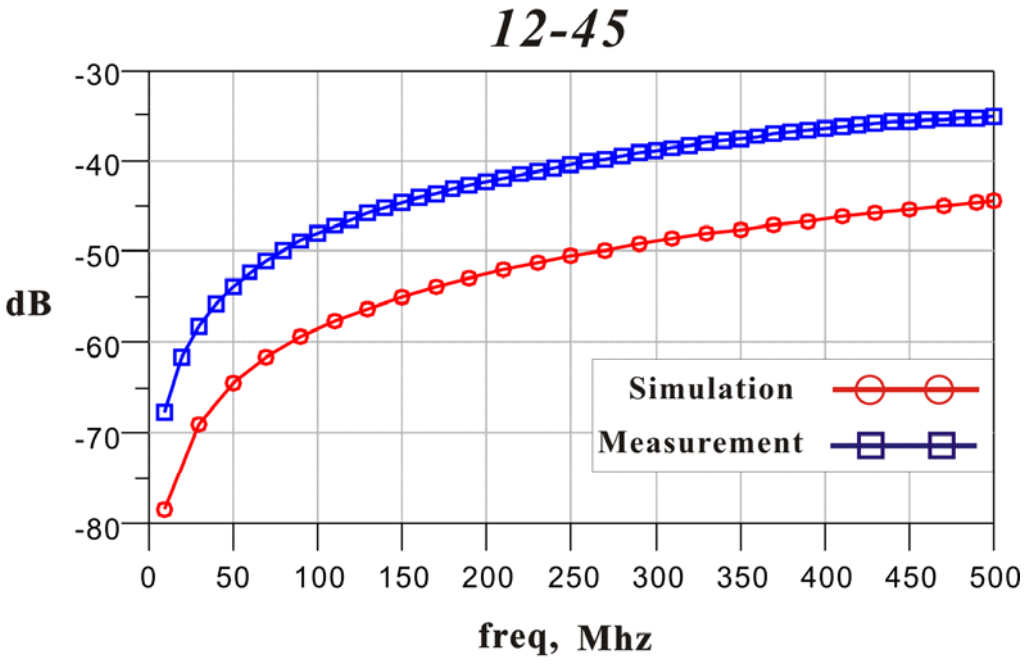
TABLE.V

S-parameter	
Start	10 MHz
Stop	500 MHz
Step	10 MHz
Z	50 Ohm
Balun	
Turn	1.414



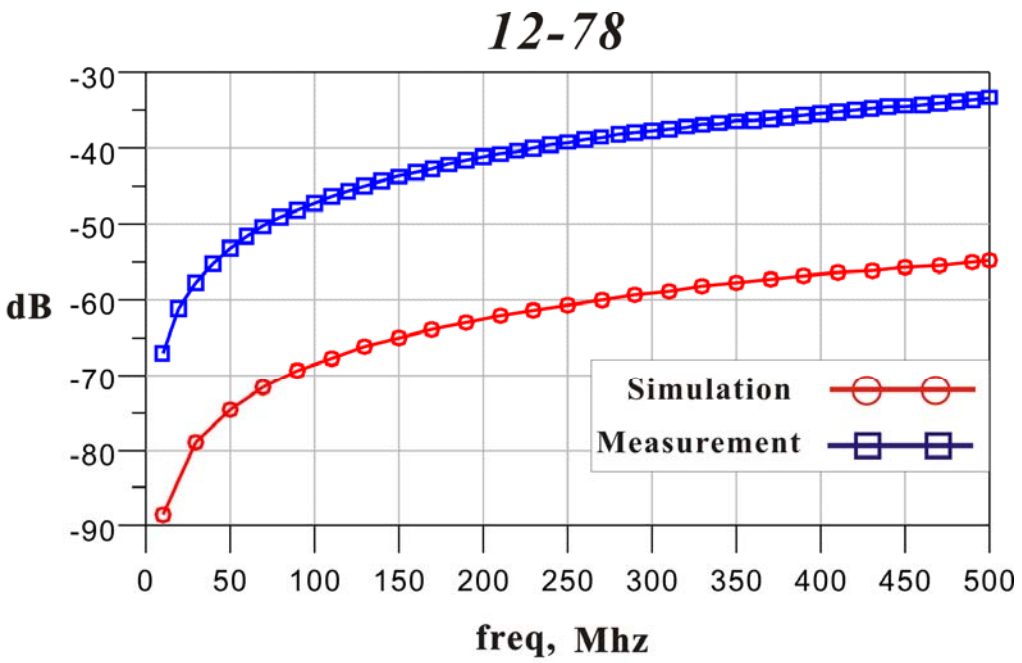
	Simulation	Measurement
250 (Mhz)	-56.6 dB	-47.7 dB

Fig.4.3.2



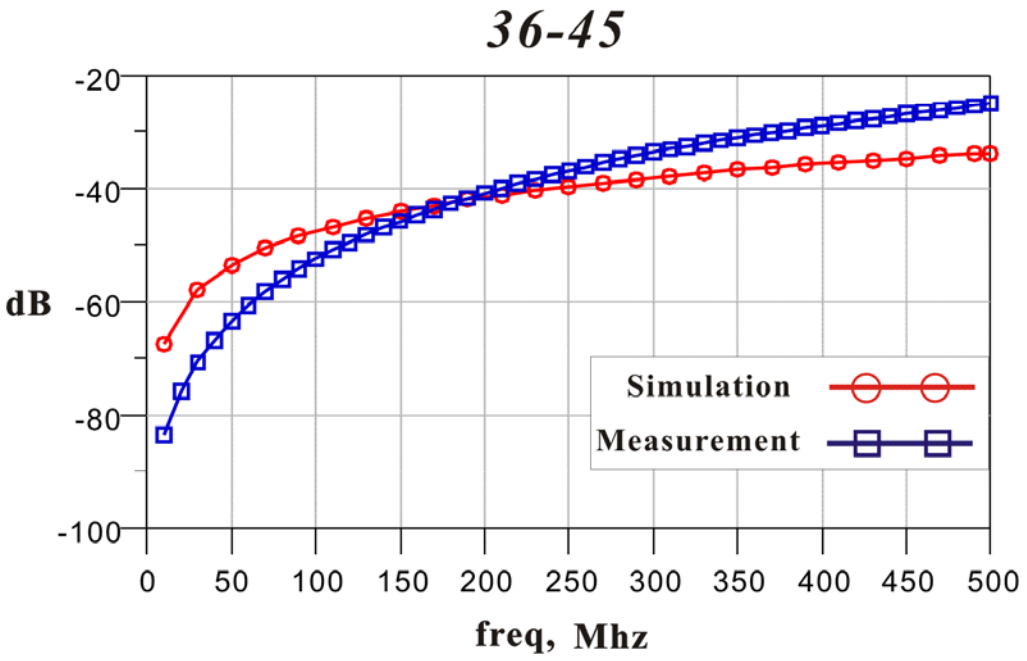
	Simulation	Measurement
250 (Mhz)	-50.53 dB	-40.49 dB

Fig.4.3.3



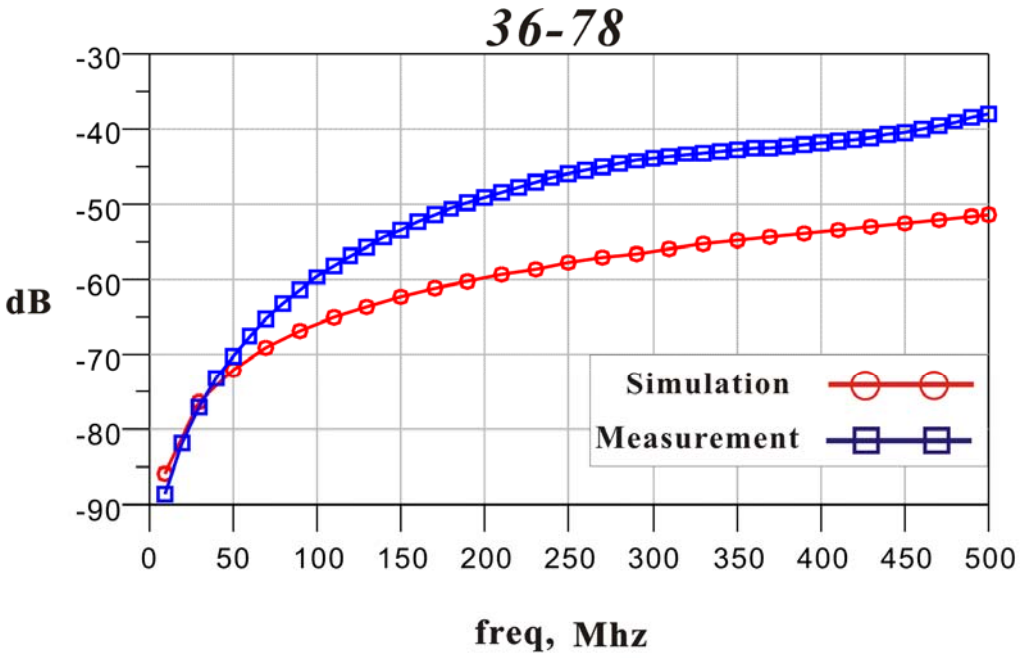
	Simulation	Measurement
250 (Mhz)	-60.69 dB	-39.25 dB

Fig.4.3.4



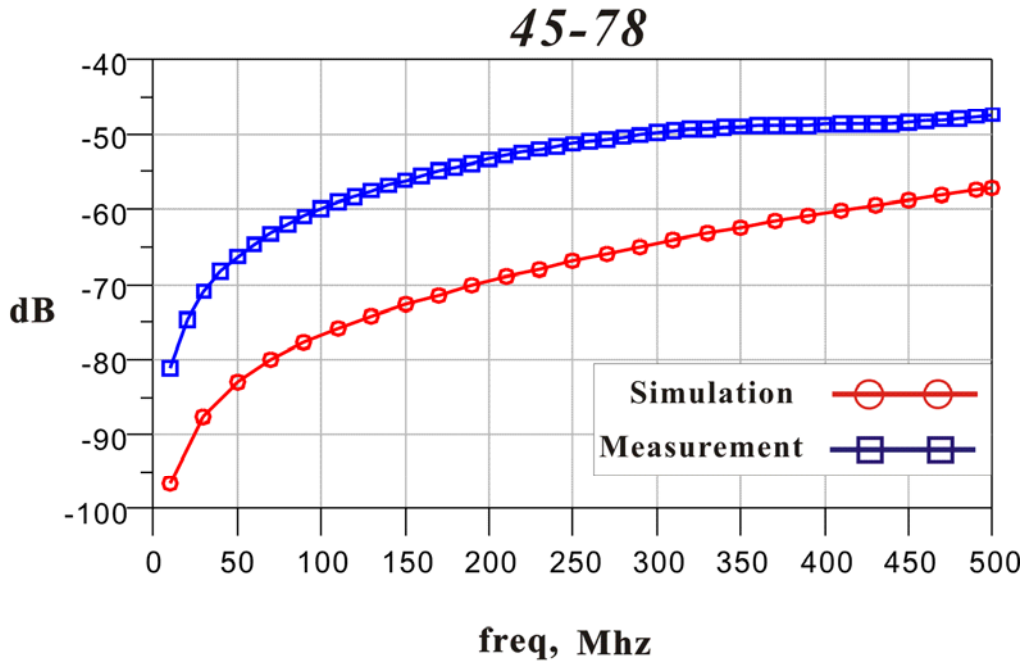
	Simulation	Measurement
250 (Mhz)	-39.75 dB	-36.99 dB

Fig.4.3.5



	Simulation	Measurement
250 (Mhz)	-57.8 dB	-45.97 dB

Fig.4.3.6



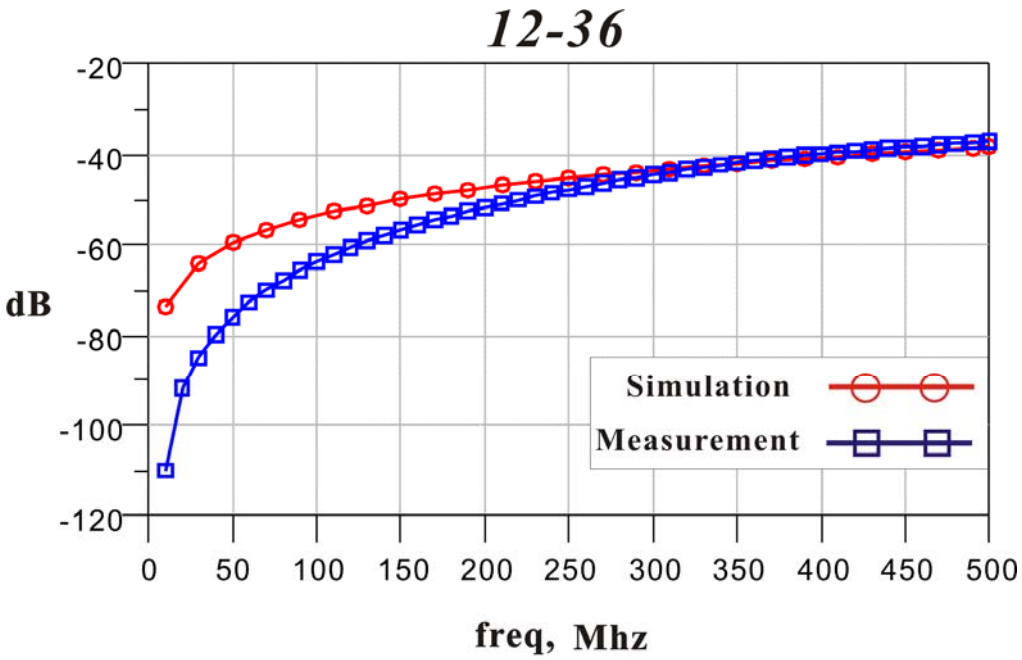
	Simulation	Measurement
250 (Mhz)	-66.9 dB	-51.32 dB

Fig.4.3.7

The results of simulation and measurement show that the tendency of the curve is similar but the amplitude is different, because the environment of simulation is too ideal. In order to match the result, we add other effects into consideration. Obviously, the interferences are from the measurement system consists of many components which cause the effects, and the crosstalk from the four pair in the untwisted region. These effects can be represented by equivalent capacitance or inductance. We add four capacitances in the simulation environment and finish the establishment of simulation by tuning to matching the curve. TABLE.VI shows the four capacitances added in the simulation environment.

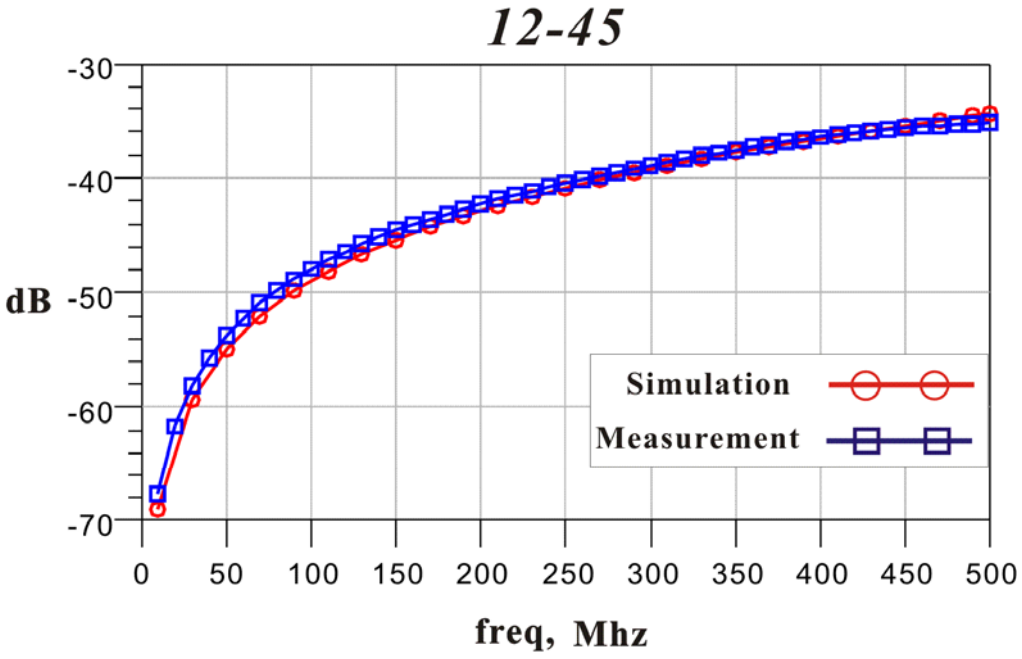
TABLE.VI

12-36			
C_{13}	C_{16}	C_{23}	C_{26}
0.2 pF	0.1 pF	0.1 pF	0.2 pF
12-45			
C_{14}	C_{15}	C_{24}	C_{25}
0.4 pF	0.55pF	0.55 pF	0.4pF
12-78			
C_{17}	C_{18}	C_{27}	C_{28}
0.4pF	0.2pF	0.2pF	0.45pF
36-45			
C_{34}	C_{35}	C_{64}	C_{65}
0.6 pF	0.1 pF	0.1 pF	0.6 pF
36-78			
C_{37}	C_{38}	C_{67}	C_{68}
0.1pF	0.25pF	0.25pF	0.1pF
45-78			
C_{47}	C_{48}	C_{57}	C_{58}
0.15 pF	0.2 pF	0.2 pF	0.1 pF



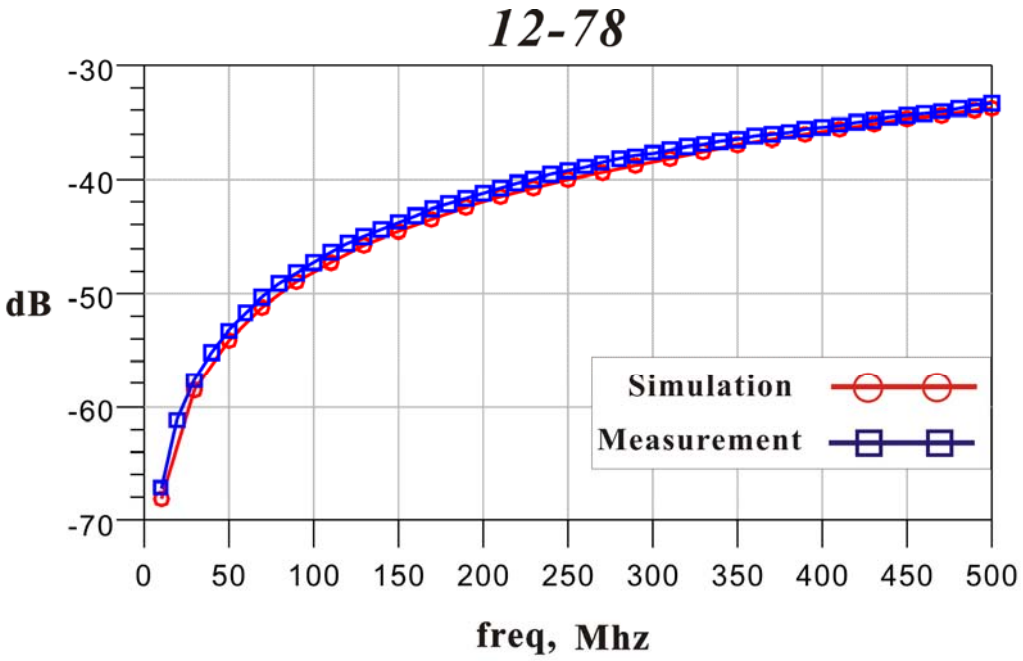
	Simulation	Measurement
250 (Mhz)	-45.3 dB	-47.7 dB

Fig.4.3.8



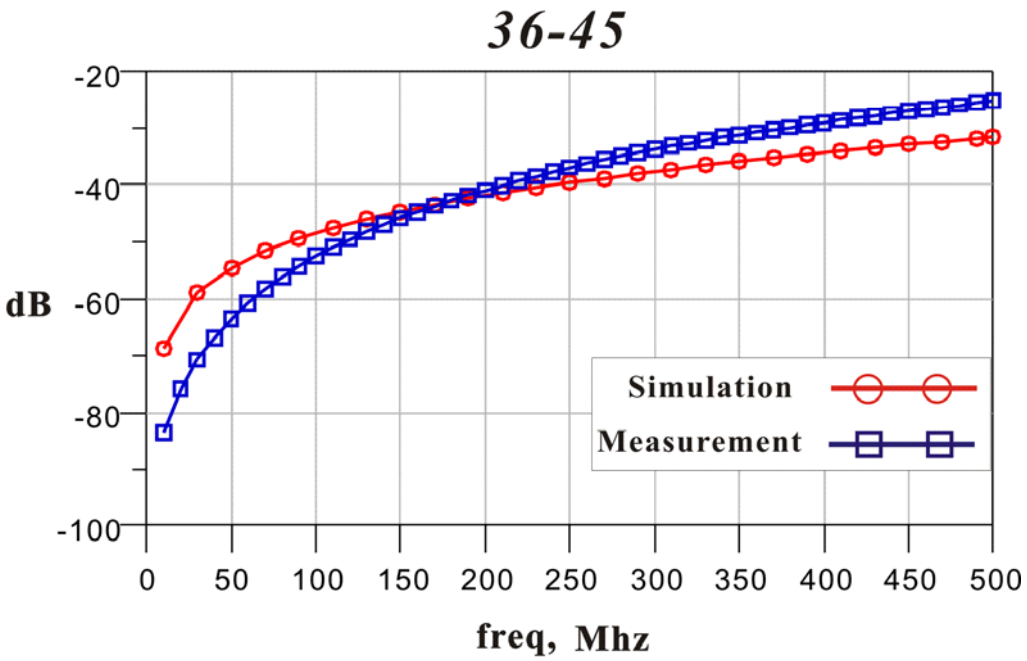
	Simulation	Measurement
250 (Mhz)	-40.88 dB	-40.49 dB

Fig.4.3.9



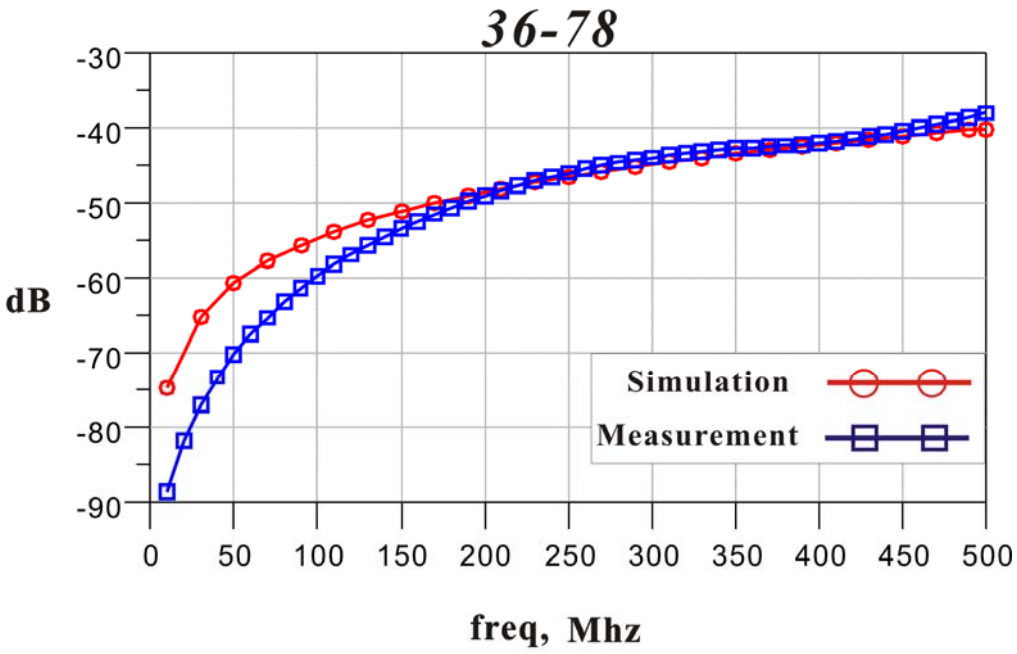
	Simulation	Measurement
250 (Mhz)	-40.09 dB	-36.25 dB

Fig.4.3.10



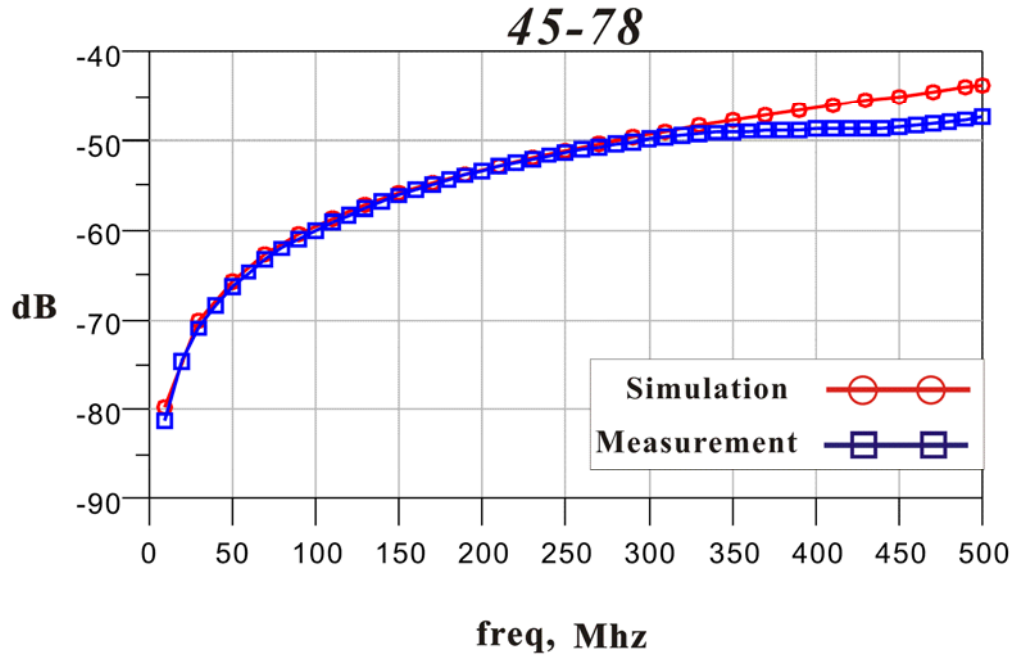
	Simulation	Measurement
250 (Mhz)	-39.6 dB	-36.99 dB

Fig.4.3.11



	Simulation	Measurement
250 (Mhz)	-46.54 dB	-45.97 dB

Fig.4.3.12



	Simulation	Measurement
250 (Mhz)	-51.14 dB	-51.32 dB

Fig.4.3.13

4.4 Compensation and the Result

In this section we use the simulation environment to compensate the capacitance on the PCB to reduce the NEXT. We don't need to calculate and compensate on the measurement system, and reduce the NEXT directly on the simulation environment. In Fig.4.4.5, the results of (12, 45) and (12, 78) do not conform the specification of EIA/TIA 568b, and we try to compensate capacitance on (12, 45) and (12, 78). Initially, we can directly regulate the capacitance of the ideal capacitor on the environment to conjecture the tendency of the NEXT loss. TABLE VII shows the result of conjecture.

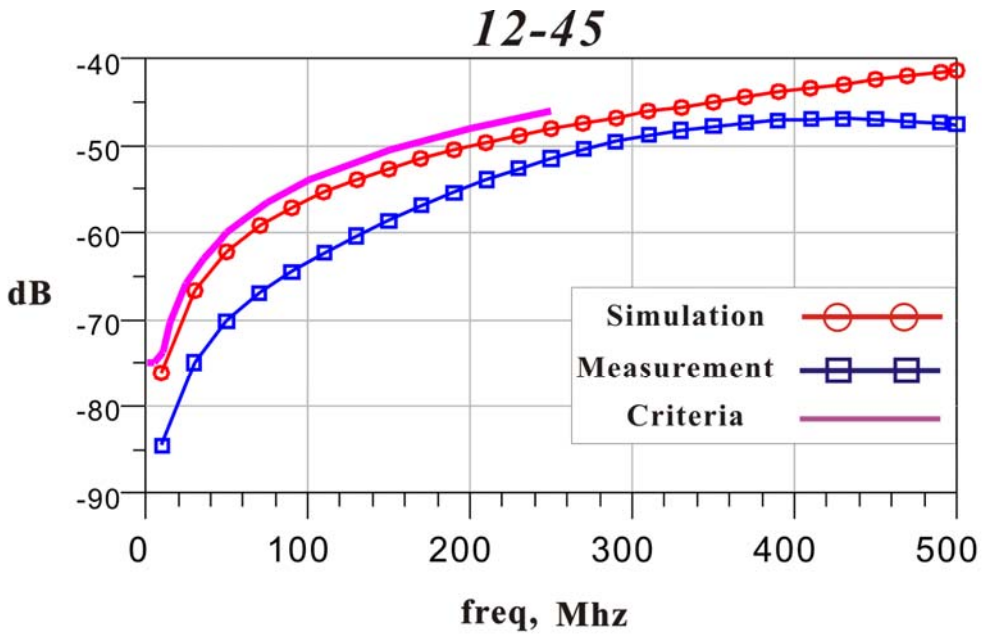
TABLE VII

(12, 45)				
Pair	C_{14}	C_{15}	C_{24}	C_{25}
change	↑	↑	↑	↑
Tendency	↓	↑	↑	↓
(12, 78)				
Pair	C_{17}	C_{18}	C_{27}	C_{28}
change	↑	↑	↑	↑
Tendency	↑	↓	↓	↑

TABLE.VIII

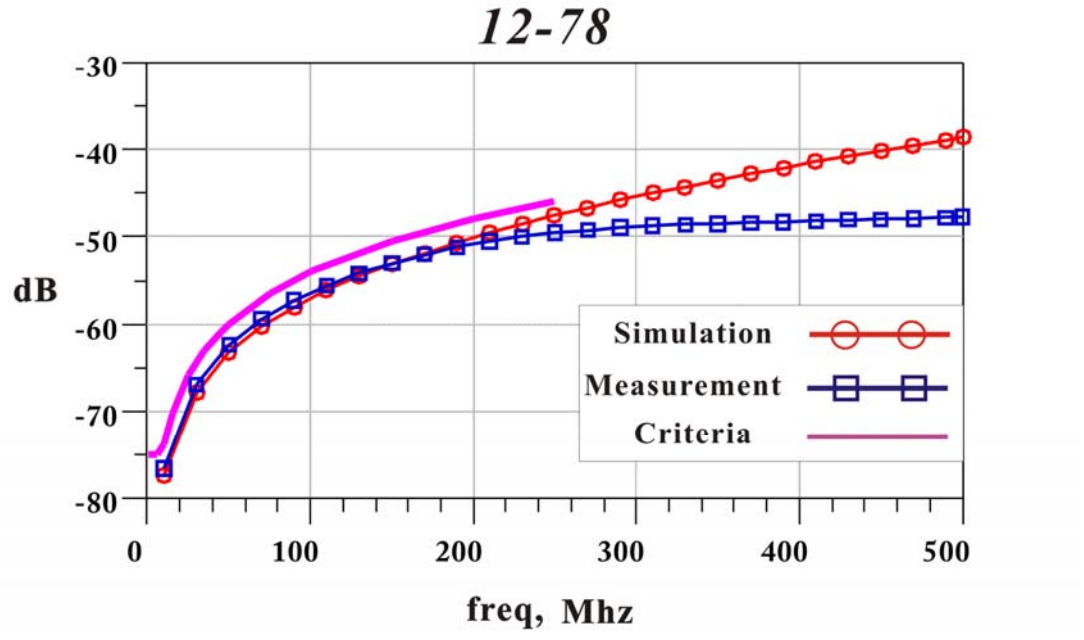
Capacitor	C_{14}	C_{25}	C_{18}
Capacitance	0.36 pF	0.33 pF	0.51 pF

The capacitors that we designed and produced in CH 3 can be used for compensating in the simulation environment. We choice the similar capacitance fallow TABLE VII, and do fine tuning. We add the capacitor between wire 1-4 and 2-5 of (12, 45) and between wire 1-8 of (12, 78). The capacitance is shown in TABLE.VIII. The result of compensating on PCB is shown in Fig.4.4.1.and Fig.4.4.2.



	Criteria	Simulation	Measurement
250 (Mhz)	-46 dB	-48.08 dB	-51.45 dB

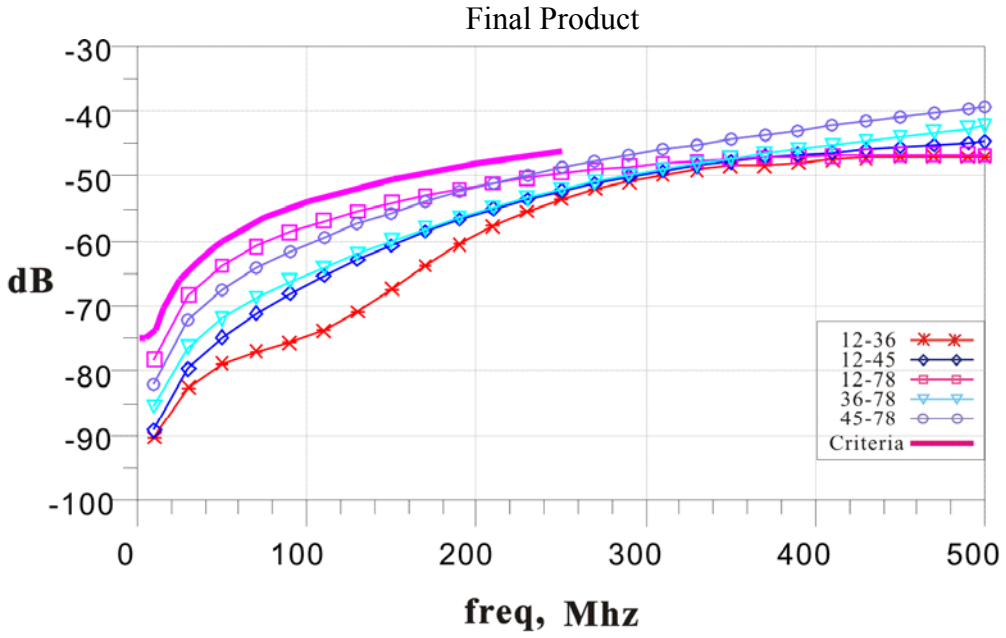
Fig.4.4.1



	Criteria	Simulation	Measurement
250 (Mhz)	-46 dB	-47.63 dB	-49.57 dB

Fig.4.4.2

The NEXT on PCB in RJ45 jack was reduced by the implementation of the balancing capacitors between the signal lines on the PCB. Fig.4.4.3 shows the results of final product. We can see that the pair (12, 36), (12, 45), (12, 78), (36, 78), (45, 78) are compensated successfully. Less than -46dB of NEXT loss was achieved at 250MHz.



	Criteria	12-36	12-45	12-78	36-78	45-78
250 (Mhz)	**-46 dB**	**-53.6 dB**	**-52.2 dB**	**-49.6 dB**	**-52.1 dB**	**-48.8 dB**

Fig.4.4.3

4.5 Conclusion

The RJ45 connector consists of many components and these components result in much interference for the transmission. Especially, it is difficult to calculate the exact capacitance compensated on PCB for balancing. To improve the method of compensation, we use ADS2006 to assist the evaluation of the crosstalk on PCB to help us calculating the capacitance and finishing the work of compensation efficiently. In this chapter, we have successfully applied the simulation environment to the design of the CAT-6 RJ45 jack. The simulation environment is successfully used to compensate the crosstalk in RJ45 connector and being validated by measurement data. More than 46 dB of NEXT loss was achieved at 250 MHz.

CHAPTER 5

CONCLUSION

Crosstalk is a critical issue in high speed transmission and connection, the method and products to reduce crosstalk noise are researched and developed. The effective method to reduce crosstalk noise recently is balancing the capacitive coupling and the inductive coupling. This balancing technique is already applied in twisted pair cable systems. In this thesis, we support the method of compensating the capacitance on PCB in Rj45 Jack for the Ethernet transmission. ADS2006A is used for evaluation. It is “Momentum” for the simulation of electromagnetic, and analyzing the effects of transmission line on PCB, and then producing the comb capacitor applied to compensating the unbalancing signal result in the capacitive crosstalk. We produce the comb capacitor and use VNA to measuring the capacitance and NEXT loss on PCB exactly, then finishing the simulation environment by utilizing the electromagnetic simulation tool for the purpose to conform the specification of CAT6 at 250MHz. The front half part introduces the basic principle of the crosstalk and the method of compensation to balancing. In order to generate the balancing signal, we should understand the situation of crosstalk between each pair of transmission line and we should take the

compensating capacitance into consideration for the best compensating result. So as to research the characteristic of the capacitors, to establish the model of comb capacitor is necessary. The length, width, thickness, and distance of the teeth are the variables, and are used to extract the characteristic of capacitor on PCB at 250MHz. From the data of measurement and simulation, the results of both are matched. Consequently, the simulated results would help us to calculate the capacitance for compensation directly. After extracting the characteristic of the capacitor on PCB, we design the transmission line on PCB and also build the simulation environment for compensation. The method of reducing crosstalk on PCB can be applied directly by using the simulation environment and be implemented on the modular jack for Ethernet transmission. These simulation works reported in this thesis is convenient and efficient for designing a compensating capacitor and a connector where the crosstalk is reduced at the frequency 250MHz.

REFERENCE

[1] A. Feller, H. R. Haupp, and J. J. Digiacomo, “Crosstalk and reflections in high-speed digital systems,” AFIPS Fall Jt. Computer Conf., vol. 27, pp. 511-525, *1965.*

[2] Paul, C.R., “Solution of the transmission-line equations under the weak-coupling assumption” *IEEE Trans. Electromagnetic Compatibility, vol. 44, no. 3, pp. 413-423, August 2002.*

[3] Namhoon Kim, “Reduction of Crosstalk Noise in Modular Jack for High-Speed Differential Signal Interconnection” *IEEE Trans. Advanced Packaging*, vol. 24, no. 3, pp. 260-267, August 2001.

[4] Joong-Guen Rhee; Sam Young Chung; Daewoo Rvu, "A study on a reduced crosstalk for the design of “CAT 6” high speed data transmission modular jack," *Environmental Electromagnetics, 2000. CEEM 2000. Proceedings. Asia-Pacific Conference on*, vol., no., pp.20-23, May, 2000.

[5] Myunghee Sung; Namhoon Kim; Junwoo Lee; Hyungsoo Kim; Baek Kyu Choi; Jae-Myun Kim; Joon-Ki Hong; Joungho Kim, "Microwave frequency crosstalk model of redistribution line patterns on wafer level package," *Advanced Packaging, IEEE Transactions on* , vol.25, no.2, pp. 265-271, May 2002

[6] Myunghee Sung; Woonghwan Ryu; Hyungsoo Kim; Jonghoon Kim; Joungho Kim, "An efficient crosstalk parameter extraction method for high-speed interconnection lines," *Advanced Packaging, IEEE Transactions on* , vol.23, no.2, pp.148-155, May 2000.

[7] Transmission Performance Specification for 4-Pair 100 Ω Category 6 Cabling: *ANSI/TIA/EIA-568-B.2-1-2002.*